USER GUIDE

multiLane

# Common Management Interface Kit

**CMIS GUI User Guide – CMIS Rev3.0/4.0 Compliant**
Revision 0.2 October 2021

**QSFP-DD Host – QSFP Host – DSFP Host – SFP-DD Host – OSFP Host**

# Notices



**General Safety Summary**

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the General Safety Summary in other system manuals for warnings and cautions related to operating the system.

**To Avoid Fire or Personal Injury**

**Use Proper Power Cord.** Only use the power cord specified for this product and certified for the country of use.

**Observe All Terminal Ratings.** To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal that exceeds the maximum rating of that terminal.

**Do Not Operate Without Covers.**

Do not operate this product with covers or panels removed.

**Avoid Exposed Circuitry.** Do not touch exposed connections and components when power is present.

**Do Not Operate with Suspected Failures.**

If you suspect there is damage to this product, have it inspected by qualified service personnel.

**Do Not Operate in Wet/Damp Conditions. Do Not Operate in an Explosive Atmosphere. Keep Product Surfaces Clean and Dry**

*Caution statements identify conditions or practices that could result in damage to this product or other property.*

# Table of Contents

# Revision Control

| Revision number | Description | Release Date |
|---|---|---|
| 0.1 | ▪ Initial version | 4/20/2020 |
| 0.22 | ▪ Added CDB Feature<br>▪ Format updates | 10/12/2021 |

# List of Acronyms

| Acronym | Definition |
|---|---|
| CMIS | Common Management Interface Kit |
| CDB | Command Data Block |
| BW | Bandwidth |
| BERT | Bit Error Rate Tester |
| Conf | Configuration |
| DUT | Device Under Test |
| FEC | Forward Error Correction |
| FW | Firmware |
| GBd | Gigabaud |
| Gbps | Gigabits per Second |
| GUI | Graphical User Interface |
| HW | Hardware |
| SI | Signal Integrity |
| Sim | Simulation |
| SW | Software |

# Introduction

The ML-CMIS GUI is a common software interface that allows to communicate with, operate and control various MCBs boards. It allows to utilize a common software across a variety of form factors.
The ML-CMIS GUI communicate with the host board through USB connection. The communication is established after installing the proper driver of the target host.
The ML-CMIS GUI allows to communicate on multiple hosts simultaneously, by assigning different USB instance to each host.

The various hosts operating with the ML-CMIS GUI are listed below:

- QDD800 host
- QDD host
- OSFP host
- QSFP host
- SFP-DD host
- DSFP host

## 1. Installation & Running

The GUI installation file is available on the website. User could download it under the target product page.

To install the GUI, simply double-click on the installer file, and follow the instructions. For Windows version newer than Windows 7 the GUI must be run as administrator. A message box will pop-up for confirmation.

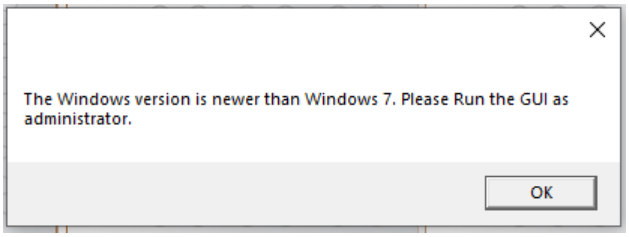


**Figure 1:** *Pop-up message*

After the GUI runs properly, a window will open as shown below.

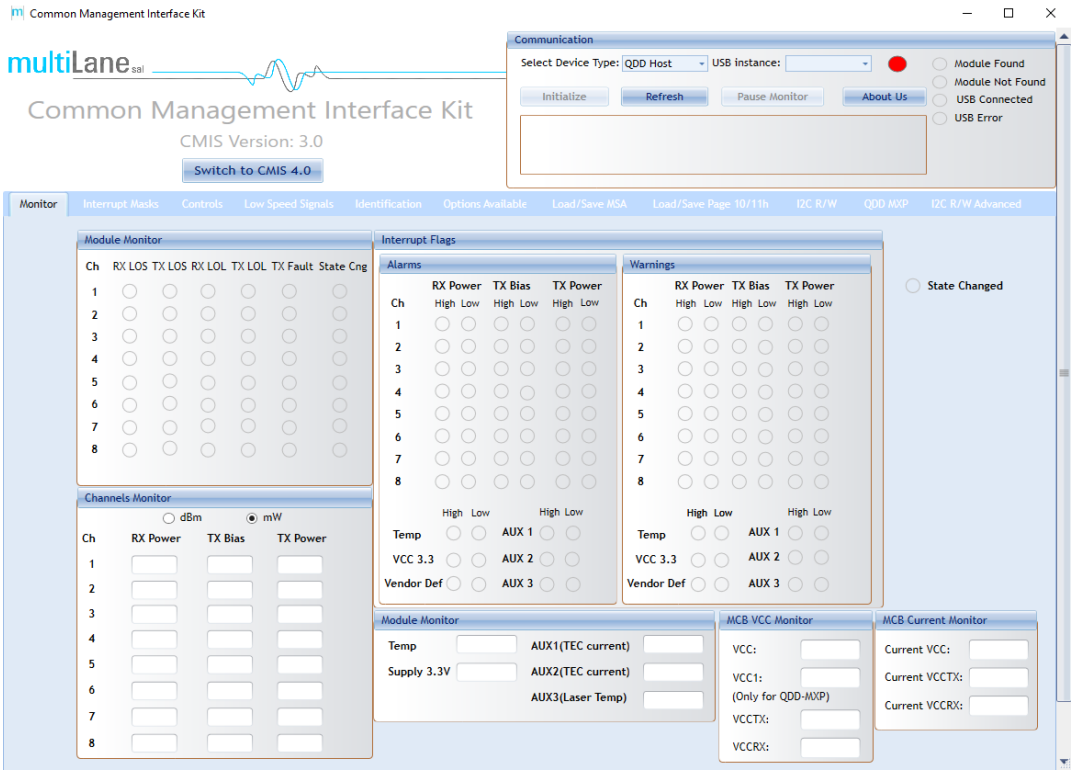


**Figure** *2*: *GUI Window*

## 2. CMIS Version

The GUI covers the CMIS 3.0 and CMIS 4.0. The user must choose the CMIS version first.

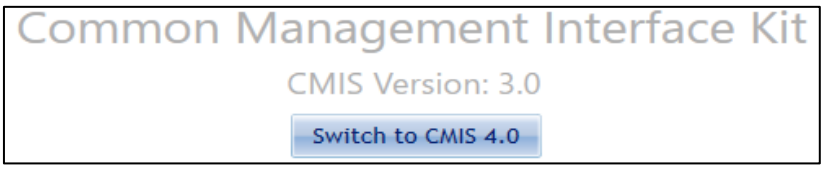


**Figure** *3*: *CMIS Version Selection*

By clicking on the button shown above, the user can switch between CMIS 3.0 and CMIS 4.0. Depending on the CMIS Version chosen by the user, the list of devices will change. Below is a summary of supported hosts based on CMIS version.

- CMIS Version 3.0
  - QDD Host
  - OSFP Hosts (ML4064-TR is under the OSFP family)
- CMIS Version 4.0
  - QDD Hosts (ML4062-TR is under the QDD family)
  - OSFP Hosts (ML4064-TR is under the OSFP family)
  - QSFP Host
  - SFP-DD Host
  - DSFP Host

## 3. Communication

The communication between the GUI and the host is established from the Communication window. Under this window, the user can select the Device Type and the USB instance.

The connection is established by clicking the Initialize button. This button is the application main entry point. Once a USB connection is established, the Host checks if a Module is inserted, and accordingly illuminates the corresponding (Module Found or Module Not Found) LED. If a Module is inserted, the initialization process proceeds with checking the related Hardware pins to ensure that the module is selected and ready to communicate with host.

Also, the following buttons are available in the Communication window.
Refresh button: Checks for connection status, refresh Hardware Readings and updates GUI.
Pause Monitor button: Pause/Resume monitoring.
About Us button: Shows software information (name, version) and company information.

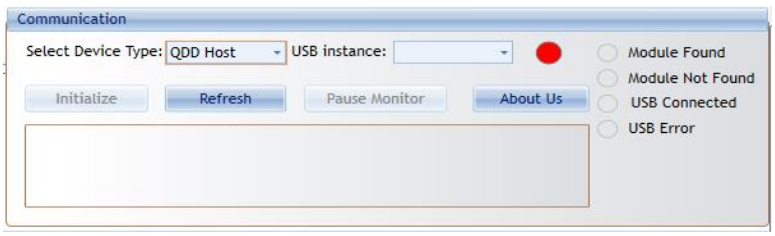


**Figure 2:** *Communication Tab*

# 4. GUI Sections

The ML-CMIS GUI contains the following tabs:

- Monitor
- Interrupt Masks
- Controls
- Low Speed Signals
- Identification
- Options Available
- Load/Save MSA
- Load/Save Page 10/11h
- I2C R/W
- I2C R/W Advanced
- DVT
- QDD-MXP (only for QSFP-DD Host)

All these tabs are common for all hosts. The subsequent sections will cover each tab separately. Any difference between various hosts in a specific tab will be mentioned explicitly.

## 4.1 Monitor

The Monitor tab shows the digital diagnostic monitoring flags status.
All alarms and warnings are expressed with LEDs as shown in Figure 5, when a flag is asserted, the corresponding LED turns ON (becomes red), when not asserted the LED remains transparent.

Also, the Monitor tab shows measurements of various monitoring values (voltage, current and temperature) and are displayed continuously.
Two main measurements windows are available:

1 - Module Monitor
2 - MCB Monitor

Note that the measured quantities differ from MCB to another depending on the implementation.

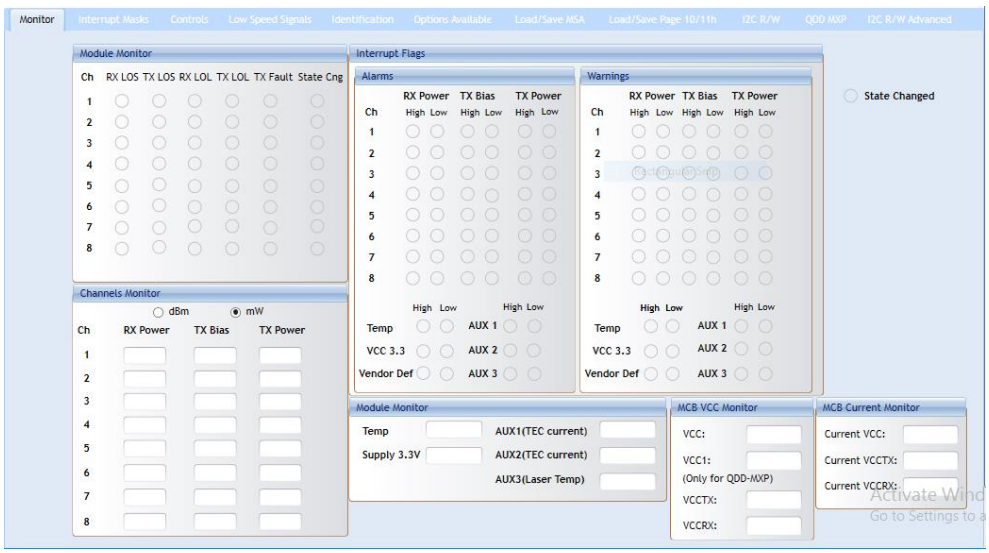


**Figure** *5*: *Monitor Tab*

The following table shows the MSA memory mapping for the monitoring tab objects.

| Byte | Bit | Name | Description | Type |
|---|---|---|---|---|
| 14 | 7-0 | Module Monitor 1: Temperature MSB | Internally measured temperature: signed 2's complement in 1/256 degree Celsius increments NOTE: Temp can be below 0. | RO Opt. |
| 15 | 7-0 | Module Monitor 1: Temperature1 LSB | | |
| 16 | 7-0 | Module Monitor 2: Supply 3.3-volt MSB | Internally measured 3.3 volt input supply voltage: in 100 µV increments | RO Opt. |
| 17 | 7-0 | Module Monitor 2: Supply 3.3-volt LSB | | |
| 18 | 7-0 | Module Monitor 3: Aux 1 MSB | TEC Current or Reserved monitor TEC Current: signed 2's complement in 1/32767% increments of maximum TEC current +32767 is max TEC current (100%) – Max Heating -32767 is min TEC current (100%) – Max Cooling | RO Opt. |
| 19 | 7-0 | Module Monitor 3: Aux 1 LSB | | |
| 20 | 7-0 | Module Monitor 4: Aux 2 MSB | TEC Current or Laser Temperature monitor TEC Current: signed 2's complement in 1/32767% increments of maximum TEC current +32767 is max TEC current (100%) – Max Heating -32767 is min TEC current (100%) – Max Cooling Laser Temperature: signed 2's complement in 1/256 degree Celsius increments See Page 01h Byte 145 Table Table 8-30 | RO Opt. |
| 21 | 7-0 | Module Monitor 4: Aux 2 LSB | | |
| 22 | 7-0 | Module Monitor 5: Aux 3 MSB | Laser Temperature or additional supply voltage monitor Laser Temperature: signed 2's complement in 1/256 degree Celsius increments Additional supply voltage monitor: in 100 µV increments See Page 01h Byte 145 Table Table 8-30 | RO Opt. |
| 23 | 7-0 | Module Monitor 5: Aux 3 LSB | | |
| 24 | 7-0 | Module Monitor 6: Custom MSB | Custom monitor | RO Opt. |
| 25 | 7-0 | Module Monitor 6: Custom LSB | | |

| | | | | |
|---|---|---|---|---|
| 8 | 7 | L-CDB block 2 complete | Latched flag to indicate completion of the CDB command for CDB block 2. Clear on Read (See Page 01h, Byte 163 bit 7) | RO Opt. |
| | 6 | L-CDB block 1 complete | Latched flag to indicate completion of the CDB command for CDB block 1. Clear on Read (See Page 01h, Byte 163 bit 6) | RO Opt. |
| | 5-3 | Reserved | | RQD |
| | 2 | Data Path firmware fault | Some modules may contain an auxiliary device for processing the transmitted and received signals (e.g. a DSP). The Data Path Firmware Fault flag becomes set when an integrity check of the firmware for this auxiliary device finds an error. | RO Opt. |
| | 1 | Module firmware fault | The Module Firmware Fault flag becomes set when an integrity check of the module firmware finds an error. There are several possible causes of the error such as program memory becoming corrupted and incomplete firmware loading. | RO Opt. |
| | 0 | L-Module state changed flag | Latched Indication of change of Module state (see Table 8-5) Clear on Read | RO RQD |
| 9 | 7 | L-Vcc3.3v Low Warning | Latched low 3.3 volts supply voltage warning flag. Clear on Read | RO Opt. |
| | 6 | L-Vcc3.3v High Warning | Latched high 3.3 volts supply voltage warning flag. Clear on Read | |
| | 5 | L-Vcc3.3v Low Alarm | Latched low 3.3 volts supply voltage alarm flag. Clear on Read | |
| | 4 | L-Vcc3.3v High Alarm | Latched high 3.3 volts supply voltage alarm flag. Clear on Read | |
| | 3 | L-Temp Low Warning | Latched low temperature warning flag. Clear on Read | |
| | 2 | L-Temp High Warning | Latched high temperature warning flag. Clear on Read | |
| | 1 | L-Temp Low Alarm | Latched low temperature alarm flag. Clear on Read | |
| | 0 | L-Temp High Alarm | Latched high temperature alarm flag. Clear on Read | |

| | | | | |
|---|---|---|---|---|
| 10 | 7 | L-Aux 2 Low Warning | Latched low warning for Aux 2 monitor. Clear on Read | RO Opt. |
| | 6 | L-Aux 2 High Warning | Latched high warning for Aux 2 monitor. Clear on Read | |
| | 5 | L-Aux 2 Low Alarm | Latched low alarm for Aux 2 monitor. Clear on Read | |
| | 4 | L-Aux 2 High Alarm | Latched high alarm for Aux 2 monitor. Clear on Read | |
| | 3 | L-Aux 1 Low Warning | Latched low warning for Aux 1 monitor. Clear on Read | |
| | 2 | L-Aux 1 High Warning | Latched high warning for Aux 1 monitor. Clear on Read | |
| | 1 | L-Aux 1 Low Alarm | Latched low alarm for Aux 1 monitor. Clear on Read | |
| | 0 | L-Aux 1 High Alarm | Latched high alarm for Aux 1 monitor. Clear on Read | |
| 11 | 7 | L-Vendor Defined Low Warning | Latched low warning for Vendor Defined Monitor. Clear on Read | RO Opt. |
| | 6 | L-Vendor Defined High Warning | Latched high warning for Vendor Defined Monitor. Clear on Read | |
| | 5 | L-Vendor Defined Low Alarm | Latched low alarm for Vendor Defined Monitor. Clear on Read | |
| | 4 | L-Vendor Defined High Alarm | Latched high alarm for Vendor Defined Monitor. Clear on Read | |
| | 3 | L-Aux 3 Low Warning | Latched low warning for Aux 3 monitor. Clear on Read | |
| | 2 | L-Aux 3 High Warning | Latched high warning for Aux 3 monitor. Clear on Read | |
| | 1 | L-Aux 3 Low Alarm | Latched low alarm for Aux 3 monitor. Clear on Read | |
| | 0 | L-Aux 3 High Alarm | Latched high alarm for Aux 3 monitor. Clear on Read | |
| 12 | 7-0 | Reserved | | |
| 13 | 7-0 | Custom | | |

| Byte | Bit | Name | Description | Type |
|---|---|---|---|---|
| 134 | 7 | L-Data Path State Changed flag, host lane 8 | Latched Data Path State Changed flag for host lane 8 | RO/COR RQD |
| | 6 | L-Data Path State changed flag, host lane 7 | Latched Data Path State Changed flag for host lane 7 | |
| | 5 | L-Data Path State Changed flag, host lane 6 | Latched Data Path State Changed flag for host lane 6 | |
| | 4 | L-Data Path State Changed flag, host lane 5 | Latched Data Path State Changed flag for host lane 5 | |
| | 3 | L-Data Path State Changed flag, host lane 4 | Latched Data Path State Changed flag for host lane 4 | |
| | 2 | L-Data Path State Changed flag, host lane 3 | Latched Data Path State Changed flag for host lane 3 | |
| | 1 | L-Data Path State Changed flag, host lane 2 | Latched Data Path State Changed flag for host lane 2 | |
| | 0 | L-Data Path State Changed flag, host lane 1 | Latched Data Path State Changed flag for host lane 1 | |
| 135 | 7 | L-Tx8 Fault flag | Latched Tx Fault flag, media lane 8 | RO Opt. |
| | 6 | L-Tx7 Fault flag | Latched Tx Fault flag, media lane 7 | |
| | 5 | L-Tx6 Fault flag | Latched Tx Fault flag, media lane 6 | |
| | 4 | L-Tx5 Fault flag | Latched Tx Fault flag, media lane 5 | |
| | 3 | L-Tx4 Fault flag | Latched Tx Fault flag, media lane 4 | |
| | 2 | L-Tx3 Fault flag | Latched Tx Fault flag, media lane 3 | |
| | 1 | L-Tx2 Fault flag | Latched Tx Fault flag, media lane 2 | |
| | 0 | L-Tx1 Fault flag | Latched Tx Fault flag, media lane 1 | |
| 136 | 7 | L-Tx8 LOS flag | Latched Tx LOS flag, lane 8 | RO Opt. |
| | 6 | L-Tx7 LOS flag | Latched Tx LOS flag, lane 7 | |
| | 5 | L-Tx6 LOS flag | Latched Tx LOS flag, lane 6 | |
| | 4 | L-Tx5 LOS flag | Latched Tx LOS flag, lane 5 | |
| | 3 | L-Tx4 LOS flag | Latched Tx LOS flag, lane 4 | |
| | 2 | L-Tx3 LOS flag | Latched Tx LOS flag, lane 3 | |
| | 1 | L-Tx2 LOS flag | Latched Tx LOS flag, lane 2 | |
| | 0 | L-Tx1 LOS flag | Latched Tx LOS flag, lane 1 | |
| 137 | 7 | L-Tx8 CDR LOL flag | Latched Tx CDR LOL flag, lane 8. Clear on Read | RO |

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|---|---|---|---|---|
| | 6 | L-Tx7 CDR LOL flag | Latched Tx CDR LOL flag, lane 7. Clear on Read | Opt. |
| | 5 | L-Tx6 CDR LOL flag | Latched Tx CDR LOL flag, lane 6. Clear on Read | |
| | 4 | L-Tx5 CDR LOL flag | Latched Tx CDR LOL flag, lane 5. Clear on Read | |
| | 3 | L-Tx4 CDR LOL flag | Latched Tx CDR LOL flag, lane 4. Clear on Read | |
| | 2 | L-Tx3 CDR LOL flag | Latched Tx CDR LOL flag, lane 3. Clear on Read | |
| | 1 | L-Tx2 CDR LOL flag | Latched Tx CDR LOL flag, lane 2. Clear on Read | |
| | 0 | L-Tx1 CDR LOL flag | Latched Tx CDR LOL flag, lane 1. Clear on Read | |
| 138 | 7 | L-Tx8 Adaptive Input Eq Fault Lane 8 flag | Latched Tx Adaptive Input Eq. Fault Lane 8. Clear on Read | RO Opt. |
| | 6 | L-Tx7 Adaptive Input Eq Fault Lane 7 flag | Latched Tx Adaptive Input Eq. Fault Lane 7. Clear on Read | |
| | 5 | L-Tx6 Adaptive Input Eq Fault Lane 6 flag | Latched Tx Adaptive Input Eq. Fault Lane 6. Clear on Read | |
| | 4 | L-Tx5 Adaptive Input Eq Fault Lane 5 flag | Latched Tx Adaptive Input Eq. Fault Lane 5. Clear on Read | |
| | 3 | L-Tx4 Adaptive Input Eq Fault Lane 4 flag | Latched Tx Adaptive Input Eq. Fault Lane 4. Clear on Read | |
| | 2 | L-Tx3 Adaptive Input Eq Fault Lane 3 flag | Latched Tx Adaptive Input Eq. Fault Lane 3. Clear on Read | |
| | 1 | L-Tx2 Adaptive Input Eq Fault Lane 2 flag | Latched Tx Adaptive Input Eq. Fault Lane 2. Clear on Read | |
| | 0 | L-Tx1 Adaptive Input Eq Fault Lane 1 flag | Latched Tx Adaptive Input Eq. Fault Lane 1. Clear on Read | |
| 139 | 7 | L-Tx8 Power High alarm | Tx output power High Alarm, media lane 8. Clear on Read | RO Opt. |
| | 6 | L-Tx7 Power High alarm | Tx output power High Alarm, media lane 7. Clear on Read | |
| | 5 | L-Tx6 Power High alarm | Tx output power High Alarm, media lane 6. Clear on Read | |
| | 4 | L-Tx5 Power High alarm | Tx output power High Alarm, media lane 5. Clear on Read | |
| | 3 | L-Tx4 Power High alarm | Tx output power High Alarm, media lane 4. Clear on Read | |
| | 2 | L-Tx3 Power High alarm | Tx output power High Alarm, media lane 3. Clear on Read | |
| | 1 | L-Tx2 Power High alarm | Tx output power High Alarm, media lane 2. Clear on Read | |
| | 0 | L-Tx1 Power High alarm | Tx output power High Alarm, media lane 1. Clear on Read | |
| 140 | 7 | L-Tx8 Power Low alarm | Tx output power Low alarm, media lane 8. Clear on Read | RO Opt. |
| | 6 | L-Tx7 Power Low alarm | Tx output power Low alarm, media lane 7. Clear on Read | |
| | 5 | L-Tx6 Power Low alarm | Tx output power Low alarm, media lane 6. Clear on Read | |
| | 4 | L-Tx5 Power Low alarm | Tx output power Low alarm, media lane 5. Clear on Read | |
| | 3 | L-Tx4 Power Low alarm | Tx output power Low alarm, media lane 4. Clear on Read | |
| | 2 | L-Tx3 Power Low alarm | Tx output power Low alarm, media lane 3. Clear on Read | |
| | 1 | L-Tx2 Power Low alarm | Tx output power Low alarm, media lane 2. Clear on Read | |
| | 0 | L-Tx1 Power Low alarm | Tx output power Low alarm, media lane 1. Clear on Read | |
| 141 | 7 | L-Tx8 Power High warning | Tx output power High warning, media lane 8. Clear on Read | RO Opt. |
| | 6 | L-Tx7 Power High warning | Tx output power High warning, media lane 7. Clear on Read | |
| | 5 | L-Tx6 Power High warning | Tx output power High warning, media lane 6. Clear on Read | |
| | 4 | L-Tx5 Power High warning | Tx output power High warning, media lane 5. Clear on Read | |
| | 3 | L-Tx4 Power High warning | Tx output power High warning, media lane 4. Clear on Read | |
| | 2 | L-Tx3 Power High warning | Tx output power High warning, media lane 3. Clear on Read | |
| | 1 | L-Tx2 Power High warning | Tx output power High warning, media lane 2. Clear on Read | |
| | 0 | L-Tx1 Power High warning | Tx output power High warning, media lane 1. Clear on Read | |
| 142 | 7 | L-Tx8 Power Low warning | Tx output power Low warning, media lane 8. Clear on Read | RO Opt. |
| | 6 | L-Tx7 Power Low warning | Tx output power Low warning, media lane 7. Clear on Read | |
| | 5 | L-Tx6 Power Low warning | Tx output power Low warning, media lane 6. Clear on Read | |
| | 4 | L-Tx5 Power Low warning | Tx output power Low warning, media lane 5. Clear on Read | |

| | | | | |
|---|---|---|---|---|
| | 3 | L-Tx4 Power Low warning | Tx output power Low warning, media lane 4. Clear on Read | |
| | 2 | L-Tx3 Power Low warning | Tx output power Low warning, media lane 3. Clear on Read | |
| | 1 | L-Tx2 Power Low warning | Tx output power Low warning, media lane 2. Clear on Read | |
| | 0 | L-Tx1 Power Low warning | Tx output power Low warning, media lane 1. Clear on Read | |
| 143 | 7 | L-Tx8 Bias High Alarm | Tx Bias High Alarm, media lane 8. Clear on Read | RO Opt. |
| | 6 | L-Tx7 Bias High Alarm | Tx Bias High Alarm, media lane 7. Clear on Read | |
| | 5 | L-Tx6 Bias High Alarm | Tx Bias High Alarm, media lane 6. Clear on Read | |
| | 4 | L-Tx5 Bias High Alarm | Tx Bias High Alarm, media lane 5. Clear on Read | |
| | 3 | L-Tx4 Bias High Alarm | Tx Bias High Alarm, media lane 4. Clear on Read | |
| | 2 | L-Tx3 Bias High Alarm | Tx Bias High Alarm, media lane 3. Clear on Read | |
| | 1 | L-Tx2 Bias High Alarm | Tx Bias High Alarm, media lane 2. Clear on Read | |
| | 0 | L-Tx1 Bias High Alarm | Tx Bias High Alarm, media lane 1. Clear on Read | |
| 144 | 7 | L-Tx8 Bias Low alarm | Tx Bias Low alarm, media lane 8. Clear on Read | RO Opt. |
| | 6 | L-Tx7 Bias Low alarm | Tx Bias Low alarm, media lane 7. Clear on Read | |
| | 5 | L-Tx6 Bias Low alarm | Tx Bias Low alarm, media lane 6. Clear on Read | |
| | 4 | L-Tx5 Bias Low alarm | Tx Bias Low alarm, media lane 5. Clear on Read | |
| | 3 | L-Tx4 Bias Low alarm | Tx Bias Low alarm, media lane 4. Clear on Read | |
| | 2 | L-Tx3 Bias Low alarm | Tx Bias Low alarm, media lane 3. Clear on Read | |
| | 1 | L-Tx2 Bias Low alarm | Tx Bias Low alarm, media lane 2. Clear on Read | |
| | 0 | L-Tx1 Bias Low alarm | Tx Bias Low alarm, media lane 1. Clear on Read | |
| 145 | 7 | L-Tx8 Bias High warning | Tx Bias High warning, media lane 8. Clear on Read | RO Opt. |
| | 6 | L-Tx7 Bias High warning | Tx Bias High warning, media lane 7. Clear on Read | |
| | 5 | L-Tx6 Bias High warning | Tx Bias High warning, media lane 6. Clear on Read | |
| | 4 | L-Tx5 Bias High warning | Tx Bias High warning, media lane 5. Clear on Read | |
| | 3 | L-Tx4 Bias High warning | Tx Bias High warning, media lane 4. Clear on Read | |
| | 2 | L-Tx3 Bias High warning | Tx Bias High warning, media lane 3. Clear on Read | |
| | 1 | L-Tx2 Bias High warning | Tx Bias High warning, media lane 2. Clear on Read | |
| | 0 | L-Tx1 Bias High warning | Tx Bias High warning, media lane 1. Clear on Read | |
| 146 | 7 | L-Tx8 Bias Low warning | Tx Bias Low warning, media lane 8. Clear on Read | RO Opt. |
| | 6 | L-Tx7 Bias Low warning | Tx Bias Low warning, media lane 7. Clear on Read | |
| | 5 | L-Tx6 Bias Low warning | Tx Bias Low warning, media lane 6. Clear on Read | |
| | 4 | L-Tx5 Bias Low warning | Tx Bias Low warning, media lane 5. Clear on Read | |
| | 3 | L-Tx4 Bias Low warning | Tx Bias Low warning, media lane 4. Clear on Read | |
| | 2 | L-Tx3 Bias Low warning | Tx Bias Low warning, media lane 3. Clear on Read | |
| | 1 | L-Tx2 Bias Low warning | Tx Bias Low warning, media lane 2. Clear on Read | |
| | 0 | L-Tx1 Bias Low warning | Tx Bias Low warning, media lane 1. Clear on Read | |
| 147 | 7 | L-Rx8 LOS | Latched Rx LOS flag, media lane 8. Clear on Read | RO Opt. |
| | 6 | L-Rx7 LOS | Latched Rx LOS flag, media lane 7. Clear on Read | |
| | 5 | L-Rx6 LOS | Latched Rx LOS flag, media lane 6. Clear on Read | |
| | 4 | L-Rx5 LOS | Latched Rx LOS flag, media lane 5. Clear on Read | |
| | 3 | L-Rx4 LOS | Latched Rx LOS flag, media lane 4. Clear on Read | |
| | 2 | L-Rx3 LOS | Latched Rx LOS flag, media lane 3. Clear on Read | |
| | 1 | L-Rx2 LOS | Latched Rx LOS flag, media lane 2. Clear on Read | |
| | 0 | L-Rx1 LOS | Latched Rx LOS flag, media lane 1. Clear on Read | |
| 148 | 7 | L-Rx8 CDR LOL | Latched Rx CDR LOL flag, media lane 8. Clear on Read | RO Opt. |
| | 6 | L-Rx7 CDR LOL | Latched Rx CDR LOL flag, media lane 7. Clear on Read | |
| | 5 | L-Rx6 CDR LOL | Latched Rx CDR LOL flag, media lane 6. Clear on Read | |
| | 4 | L-Rx5 CDR LOL | Latched Rx CDR LOL flag, media lane 5. Clear on Read | |
| | 3 | L-Rx4 CDR LOL | Latched Rx CDR LOL flag, media lane 4. Clear on Read | |

| | | | | |
|---|---|---|---|---|
| | 2 | L-Rx3 CDR LOL | Latched Rx CDR LOL flag, media lane 3. Clear on Read | |
| | 1 | L-Rx2 CDR LOL | Latched Rx CDR LOL flag, media lane 2. Clear on Read | |
| | 0 | L-Rx1 CDR LOL | Latched Rx CDR LOL flag, media lane 1. Clear on Read | |
| 149 | 7 | L-Rx8 Power High alarm | Rx input power High alarm, media lane 8. Clear on Read | RO Opt. |
| | 6 | L-Rx7 Power High alarm | Rx input power High alarm, media lane 7. Clear on Read | |
| | 5 | L-Rx6 Power High alarm | Rx input power High alarm, media lane 6. Clear on Read | |
| | 4 | L-Rx5 Power High alarm | Rx input power High alarm, media lane 5. Clear on Read | |
| | 3 | L-Rx4 Power High alarm | Rx input power High alarm, media lane 4. Clear on Read | |
| | 2 | L-Rx3 Power High alarm | Rx input power High alarm, media lane 3. Clear on Read | |
| | 1 | L-Rx2 Power High alarm | Rx input power High alarm, media lane 2. Clear on Read | |
| | 0 | L-Rx1 Power High alarm | Rx input power High alarm, media lane 1. Clear on Read | |
| 150 | 7 | L-Rx8 Power Low alarm | Rx input power Low alarm, media lane 8. Clear on Read | RO Opt. |
| | 6 | L-Rx7 Power Low alarm | Rx input power Low alarm, media lane 7. Clear on Read | |
| | 5 | L-Rx6 Power Low alarm | Rx input power Low alarm, media lane 6. Clear on Read | |
| | 4 | L-Rx5 Power Low alarm | Rx input power Low alarm, media lane 5. Clear on Read | |
| | 3 | L-Rx4 Power Low alarm | Rx input power Low alarm, media lane 4. Clear on Read | |
| | 2 | L-Rx3 Power Low alarm | Rx input power Low alarm, media lane 3. Clear on Read | |
| | 1 | L-Rx2 Power Low alarm | Rx input power Low alarm, media lane 2. Clear on Read | |
| | 0 | L-Rx1 Power Low alarm | Rx input power Low alarm, media lane 1. Clear on Read | |
| 151 | 7 | L-Rx8 Power High warning | Rx input power High warning, media lane 8. Clear on Read | RO Opt. |
| | 6 | L-Rx7 Power High warning | Rx input power High warning, media lane 7. Clear on Read | |
| | 5 | L-Rx6 Power High warning | Rx input power High warning, media lane 6. Clear on Read | |
| | 4 | L-Rx5 Power High warning | Rx input power High warning, media lane 5. Clear on Read | |
| | 3 | L-Rx4 Power High warning | Rx input power High warning, media lane 4. Clear on Read | |
| | 2 | L-Rx3 Power High warning | Rx input power High warning, media lane 3. Clear on Read | |
| | 1 | L-Rx2 Power High warning | Rx input power High warning, media lane 2. Clear on Read | |
| | 0 | L-Rx1 Power High warning | Rx input power High warning, media lane 1. Clear on Read | |
| 152 | 7 | L-Rx8 Power Low warning | Rx input power Low warning, media lane 8. Clear on Read | RO Opt. |
| | 6 | L-Rx7 Power Low warning | Rx input power Low warning, media lane 7. Clear on Read | |
| | 5 | L-Rx6 Power Low warning | Rx input power Low warning, media lane 6. Clear on Read | |
| | 4 | L-Rx5 Power Low warning | Rx input power Low warning, media lane 5. Clear on Read | |
| | 3 | L-Rx4 Power Low warning | Rx input power Low warning, media lane 4. Clear on Read | |
| | 2 | L-Rx3 Power Low warning | Rx input power Low warning, media lane 3. Clear on Read | |
| | 1 | L-Rx2 Power Low warning | Rx input power Low warning, media lane 2. Clear on Read | |
| | 0 | L-Rx1 Power Low warning | Rx input power Low warning, media lane 1. Clear on Read | |

| Byte | Bit | Name | Description | Type |
|---|---|---|---|---|
| 153 | 7-0 | Reserved | | RO |
| 154 | 7-0 | Tx1 Power MSB | Internally measured Tx output optical power: unsigned integer in 0.1 uW increments, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm) | RO Opt. |
| 155 | 7-0 | Tx1 Power LSB | | |
| 156 | 7-0 | Tx2 Power MSB | | |
| 157 | 7-0 | Tx2 Power LSB | | |
| 158 | 7-0 | Tx3 Power MSB | | |
| 159 | 7-0 | Tx3 Power LSB | | |
| 160 | 7-0 | Tx4 Power MSB | | |
| 161 | 7-0 | Tx4 Power LSB | | |
| 162 | 7-0 | Tx5 Power MSB | | |
| 163 | 7-0 | Tx5 Power LSB | | |
| 164 | 7-0 | Tx6 Power MSB | | |
| 165 | 7-0 | Tx6 Power LSB | | |
| 166 | 7-0 | Tx7 Power MSB | | |
| 167 | 7-0 | Tx7 Power LSB | | |
| 168 | 7-0 | Tx8 Power MSB | | |
| 169 | 7-0 | Tx8 Power LSB | | |

| | | | | |
|---|---|---|---|---|
| 170 | 7-0 | Tx1 Bias MSB | Internally measured Tx bias current monitor: unsigned integer in 2 uA increments, times the multiplier from Table 8-33. | RO Opt. |
| 171 | 7-0 | Tx1 Bias LSB | | |
| 172 | 7-0 | Tx2 Bias MSB | | |
| 173 | 7-0 | Tx2 Bias LSB | | |
| 174 | 7-0 | Tx3 Bias MSB | | |
| 175 | 7-0 | Tx3 Bias LSB | | |
| 176 | 7-0 | Tx4 Bias MSB | | |
| 177 | 7-0 | Tx4 Bias LSB | | |
| 178 | 7-0 | Tx5 Bias MSB | | |
| 179 | 7-0 | Tx5 Bias LSB | | |
| 180 | 7-0 | Tx6 Bias MSB | | |
| 181 | 7-0 | Tx6 Bias LSB | | |
| 182 | 7-0 | Tx7 Bias MSB | | |
| 183 | 7-0 | Tx7 Bias LSB | | |
| 184 | 7-0 | Tx8 Bias MSB | | |
| 185 | 7-0 | Tx8 Bias LSB | | |
| 186 | 7-0 | Rx1 Power MSB | Internally measured Rx input optical power: unsigned integer in 0.1 uW increments, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm) | RO Opt. |
| 187 | 7-0 | Rx1 Power LSB | | |
| 188 | 7-0 | Rx2 Power MSB | | |
| 189 | 7-0 | Rx2 Power LSB | | |
| 190 | 7-0 | Rx3 Power MSB | | |
| 191 | 7-0 | Rx3 Power LSB | | |
| 192 | 7-0 | Rx4 Power MSB | | |
| 193 | 7-0 | Rx4 Power LSB | | |
| 194 | 7-0 | Rx5 Power MSB | | |
| 195 | 7-0 | Rx5 Power LSB | | |
| 196 | 7-0 | Rx6 Power MSB | | |
| 197 | 7-0 | Rx6 Power LSB | | |
| 198 | 7-0 | Rx7 Power MSB | | |
| 199 | 7-0 | Rx7 Power LSB | | |
| 200 | 7-0 | Rx8 Power MSB | | |
| 201 | 7-0 | Rx8 Power LSB | | |

## 4.2 Interrupt Masks

Masks shown in this tab are used to prevent a specified flag of generating an interrupt (IntL) when asserted and prevent continued interruption from on-going conditions.
When a mask is set, an interrupt will not be asserted by the corresponding (Alarm/Warning) latched flag bit.
All Masking bits are volatile and will be reset (set to 0) on module startup.

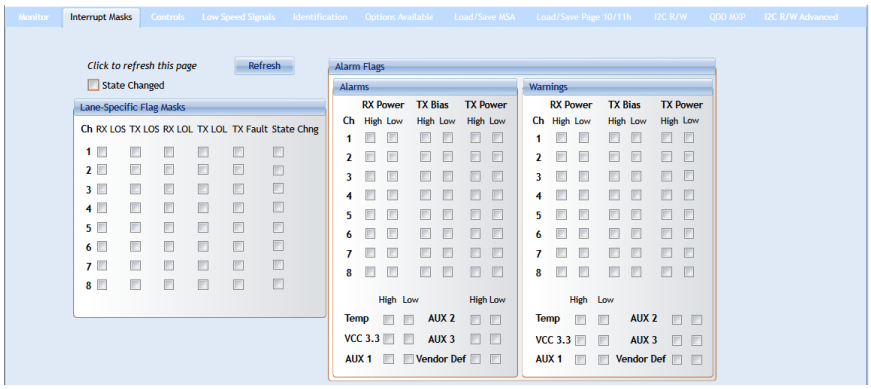


**Figure 3: Interrupt Masks Tab**

The table below shows the corresponding MSA mapping for the interrupt flags.

| Byte | Bits | Name | Description | Type |
|---|---|---|---|---|
| 213 | 7 | M- Data Path State Changed flag mask, host lane 8 | Masking bit for Data Path State Changed flag, host lane 8 | RW RQD |
| | 6 | M-Data Path State Changed flag mask, host lane 7 | Masking bit for Data Path State Changed flag, host lane 7 | |
| | 5 | M-Data Path State Changed flag mask, host lane 6 | Masking bit for Data Path State Changed flag, host lane 6 | |
| | 4 | M-Data Path State Changed flag mask, host lane 5 | Masking bit for Data Path State Changed flag, host lane 5 | |
| | 3 | M-Data Path State Changed flag mask, host lane 4 | Masking bit for Data Path State Changed flag, host lane 4 | |
| | 2 | M-Data Path State Changed flag mask, host lane 3 | Masking bit for Data Path State Changed flag, host lane 3 | |
| | 1 | M-Data Path State Changed flag mask, host lane 2 | Masking bit for Data Path State Changed flag, host lane 2 | |
| | 0 | M-Data Path State Changed flag mask, host lane 1 | Masking bit for Data Path State Changed flag, host lane 1 | |
| 214 | 7 | M-Tx8 Fault flag mask | Masking bit for Tx Fault flag, media lane 8 | RW Opt. |
| | 6 | M-Tx7 Fault flag mask | Masking bit for Tx Fault flag, media lane 7 | |
| | 5 | M-Tx6 Fault flag mask | Masking bit for Tx Fault flag, media lane 6 | |
| | 4 | M-Tx5 Fault flag mask | Masking bit for Tx Fault flag, media lane 5 | |
| | 3 | M-Tx4 Fault flag mask | Masking bit for Tx Fault flag, media lane 4 | |
| | 2 | M-Tx3 Fault flag mask | Masking bit for Tx Fault flag, media lane 3 | |
| | 1 | M-Tx2 Fault flag mask | Masking bit for Tx Fault flag, media lane 2 | |
| | 0 | M-Tx1 Fault flag mask | Masking bit for Tx Fault flag, media lane 1 | |
| 215 | 7 | M-Tx8 LOS flag mask | Masking bit for Tx LOS flag, lane 8 | RW Opt. |
| | 6 | M-Tx7 LOS flag mask | Masking bit for Tx LOS flag, lane 7 | |
| | 5 | M-Tx6 LOS flag mask | Masking bit for Tx LOS flag, lane 6 | |
| | 4 | M-Tx5 LOS flag mask | Masking bit for Tx LOS flag, lane 5 | |
| | 3 | M-Tx4 LOS flag mask | Masking bit for Tx LOS flag, lane 4 | |
| | 2 | M-Tx3 LOS flag mask | Masking bit for Tx LOS flag, lane 3 | |
| | 1 | M-Tx2 LOS flag mask | Masking bit for Tx LOS flag, lane 2 | |
| | 0 | M-Tx1 LOS flag mask | Masking bit for Tx LOS flag, lane 1 | |
| 216 | 7 | M-Tx8 CDR LOL flag mask | Masking bit for Tx CDR LOL flag, lane 8 | RW Opt. |
| | 6 | M-Tx7 CDR LOL flag mask | Masking bit for Tx CDR LOL flag, lane 7 | |
| | 5 | M-Tx6 CDR LOL flag mask | Masking bit for Tx CDR LOL flag, lane 6 | |
| | 4 | M-Tx5 CDR LOL flag mask | Masking bit for Tx CDR LOL flag, lane 5 | |
| | 3 | M-Tx4 CDR LOL flag mask | Masking bit for Tx CDR LOL flag, lane 4 | |
| | 2 | M-Tx3 CDR LOL flag mask | Masking bit for Tx CDR LOL flag, lane 3 | |
| | 1 | M-Tx2 CDR LOL flag mask | Masking bit for Tx CDR LOL flag, lane 2 | |
| | 0 | M-Tx1 CDR LOL flag mask | Masking bit for Tx CDR LOL flag, lane 1 | |
| 217 | 7 | M-Tx8 Adaptive Eq Fault flag mask | Masking bit for Tx Adaptive Input Eq Fail lane 8 | RW Opt. |
| | 6 | M-Tx7 Adaptive Eq Fault flag mask | Masking bit for Tx Adaptive Input Eq Fail lane 7 | |
| | 5 | M-Tx6 Adaptive Eq Fault flag mask | Masking bit for Tx Adaptive Input Eq Fail lane 6 | |
| | 4 | M-Tx5 Adaptive Eq Fault flag mask | Masking bit for Tx Adaptive Input Eq Fail lane 5 | |
| | 3 | M-Tx4 Adaptive Eq Fault flag mask | Masking bit for Tx Adaptive Input Eq Fail lane 4 | |
| | 2 | M-Tx3 Adaptive Eq Fault flag mask | Masking bit for Tx Adaptive Input Eq Fail lane 3 | |
| | 1 | M-Tx2 Adaptive Eq Fault flag mask | Masking bit for Tx Adaptive Input Eq Fail lane 2 | |
| | 0 | M-Tx1 Adaptive Eq Fault flag mask | Masking bit for Tx Adaptive Input Eq Fail lane 1 | |
| 218 | 7 | M-Tx8 Power High Alarm flag mask | Masking bit for Tx output power High Alarm, media lane 8 | RW Opt. |
| | 6 | M-Tx7 Power High Alarm flag mask | Masking bit for Tx output power High Alarm, media lane 7 | |

| | | | | |
|---|---|---|---|---|
| | 5 | M-Tx6 Power High Alarm flag mask | Masking bit for Tx output power High Alarm, media lane 6 | |
| | 4 | M-Tx5 Power High Alarm flag mask | Masking bit for Tx output power High Alarm, media lane 5 | |
| | 3 | M-Tx4 Power High Alarm flag mask | Masking bit for Tx output power High Alarm, media lane 4 | |
| | 2 | M-Tx3 Power High Alarm flag mask | Masking bit for Tx output power High Alarm, media lane 3 | |
| | 1 | M-Tx2 Power High Alarm flag mask | Masking bit for Tx output power High Alarm, media lane 2 | |
| | 0 | M-Tx1 Power High Alarm flag mask | Masking bit for Tx output power High Alarm, media lane 1 | |
| 219 | 7 | M-Tx8 Power Low Alarm flag mask | Masking bit for Tx output power Low Alarm, media lane 8 | RW Opt. |
| | 6 | M-Tx7 Power Low Alarm flag mask | Masking bit for Tx output power Low Alarm, media lane 7 | |
| | 5 | M-Tx6 Power Low Alarm flag mask | Masking bit for Tx output power Low Alarm, media lane 6 | |
| | 4 | M-Tx5 Power Low Alarm flag mask | Masking bit for Tx output power Low Alarm, media lane 5 | |
| | 3 | M-Tx4 Power Low Alarm flag mask | Masking bit for Tx output power Low Alarm, media lane 4 | |
| | 2 | M-Tx3 Power Low Alarm flag mask | Masking bit for Tx output power Low Alarm, media lane 3 | |
| | 1 | M-Tx2 Power Low Alarm flag mask | Masking bit for Tx output power Low Alarm, media lane 2 | |
| | 0 | M-Tx1 Power Low Alarm flag mask | Masking bit for Tx output power Low Alarm, media lane 1 | |
| 220 | 7 | M-Tx8 Power High Warning flag mask | Masking bit for Tx output power High Warning, media lane 8 | RW Opt. |
| | 6 | M-Tx7 Power High Warning flag mask | Masking bit for Tx output power High Warning, media lane 7 | |
| | 5 | M-Tx6 Power High Warning flag mask | Masking bit for Tx output power High Warning, media lane 6 | |
| | 4 | M-Tx5 Power High Warning flag mask | Masking bit for Tx output power High Warning, media lane 5 | |
| | 3 | M-Tx4 Power High Warning flag mask | Masking bit for Tx output power High Warning, media lane 4 | |
| | 2 | M-Tx3 Power High Warning flag mask | Masking bit for Tx output power High Warning, media lane 3 | |
| | 1 | M-Tx2 Power High Warning flag mask | Masking bit for Tx output power High Warning, media lane 2 | |
| | 0 | M-Tx1 Power High Warning flag mask | Masking bit for Tx output power High Warning, media lane 1 | |
| 221 | 7 | M-Tx8 Power Low Warning flag mask | Masking bit for Tx output power Low Warning, media lane 8 | RW Opt. |
| | 6 | M-Tx7 Power Low Warning flag mask | Masking bit for Tx output power Low Warning, media lane 7 | |
| | 5 | M-Tx6 Power Low Warning flag mask | Masking bit for Tx output power Low Warning, media lane 6 | |
| | 4 | M-Tx5 Power Low Warning flag mask | Masking bit for Tx output power Low Warning, media lane 5 | |
| | 3 | M-Tx4 Power Low Warning flag mask | Masking bit for Tx output power Low Warning, media lane 4 | |
| | 2 | M-Tx3 Power Low Warning flag mask | Masking bit for Tx output power Low Warning, media lane 3 | |
| | 1 | M-Tx2 Power Low Warning flag mask | Masking bit for Tx output power Low Warning, media lane 2 | |
| | 0 | M-Tx1 Power Low Warning flag mask | Masking bit for Tx output power Low Warning, media lane 1 | |
| 222 | 7 | M-Tx8 Bias High Alarm flag mask | Masking bit for Tx bias High Alarm, media lane 8 | RW Opt. |
| | 6 | M-Tx7 Bias High Alarm flag mask | Masking bit for Tx bias High Alarm, media lane 7 | |
| | 5 | M-Tx6 Bias High Alarm flag mask | Masking bit for Tx bias High Alarm, media lane 6 | |
| | 4 | M-Tx5 Bias High Alarm flag mask | Masking bit for Tx bias High Alarm, media lane 5 | |
| | 3 | M-Tx4 Bias High Alarm flag mask | Masking bit for Tx bias High Alarm, media lane 4 | |
| | 2 | M-Tx3 Bias High Alarm flag mask | Masking bit for Tx bias High Alarm, media lane 3 | |
| | 1 | M-Tx2 Bias High Alarm flag mask | Masking bit for Tx bias High Alarm, media lane 2 | |
| | 0 | M-Tx1 Bias High Alarm flag mask | Masking bit for Tx bias High Alarm, media lane 1 | |

| | | | | |
|---|---|---|---|---|
| 223 | 7 | M-Tx8 Bias Low Alarm flag mask | Masking bit for Tx bias Low Alarm, media lane 8 | RW Opt. |
| | 6 | M-Tx7 Bias Low Alarm flag mask | Masking bit for Tx bias Low Alarm, media lane 7 | |
| | 5 | M-Tx6 Bias Low Alarm flag mask | Masking bit for Tx bias Low Alarm, media lane 6 | |
| | 4 | M-Tx5 Bias Low Alarm flag mask | Masking bit for Tx bias Low Alarm, media lane 5 | |
| | 3 | M-Tx4 Bias Low Alarm flag mask | Masking bit for Tx bias Low Alarm, media lane 4 | |
| | 2 | M-Tx3 Bias Low Alarm flag mask | Masking bit for Tx bias Low Alarm, media lane 3 | |
| | 1 | M-Tx2 Bias Low Alarm flag mask | Masking bit for Tx Bias Low Alarm, media lane 2 | |
| | 0 | M-Tx1 Bias Low Alarm flag mask | Masking bit for Tx Bias Low Alarm, media lane 1 | |
| 224 | 7 | M-Tx8 Bias High Warning flag mask | Masking bit for Tx Bias High Warning, media lane 8 | RW Opt. |
| | 6 | M-Tx7 Bias High Warning flag mask | Masking bit for Tx Bias High Warning, media lane 7 | |
| | 5 | M-Tx6 Bias High Warning flag mask | Masking bit for Tx Bias High Warning, media lane 6 | |
| | 4 | M-Tx5 Bias High Warning flag mask | Masking bit for Tx Bias High Warning, media lane 5 | |
| | 3 | M-Tx4 Bias High Warning flag mask | Masking bit for Tx Bias High Warning, media lane 4 | |
| | 2 | M-Tx3 Bias High Warning flag mask | Masking bit for Tx Bias High Warning, media lane 3 | |
| | 1 | M-Tx2 Bias High Warning flag mask | Masking bit for Tx Bias High Warning, media lane 2 | |
| | 0 | M-Tx1 Bias High Warning flag mask | Masking bit for Tx Bias High Warning, media lane 1 | |
| 225 | 7 | M-Tx8 Bias Low Warning flag mask | Masking bit for Tx Bias Low Warning, media lane 8 | RW Opt. |
| | 6 | M-Tx7 Bias Low Warning flag mask | Masking bit for Tx Bias Low Warning, media lane 7 | |
| | 5 | M-Tx6 Bias Low Warning flag mask | Masking bit for Tx Bias Low Warning, media lane 6 | |
| | 4 | M-Tx5 Bias Low Warning flag mask | Masking bit for Tx Bias Low Warning, media lane 5 | |
| | 3 | M-Tx4 Bias Low Warning flag mask | Masking bit for Tx Bias Low Warning, media lane 4 | |
| | 2 | M-Tx3 Bias Low Warning flag mask | Masking bit for Tx Bias Low Warning, media lane 3 | |
| | 1 | M-Tx2 Bias Low Warning flag mask | Masking bit for Tx Bias Low Warning, media lane 2 | |
| | 0 | M-Tx1 Bias Low Warning flag mask | Masking bit for Tx Bias Low Warning, media lane 1 | |
| 226 | 7 | M-Rx8 LOS flag mask | Masking bit for Rx LOS flag, media lane 8 | RW Opt. |
| | 6 | M-Rx7 LOS flag mask | Masking bit for Rx LOS flag, media lane 7 | |
| | 5 | M-Rx6 LOS flag mask | Masking bit for Rx LOS flag, media lane 6 | |
| | 4 | M-Rx5 LOS flag mask | Masking bit for Rx LOS flag, media lane 5 | |
| | 3 | M-Rx4 LOS flag mask | Masking bit for Rx LOS flag, media lane 4 | |
| | 2 | M-Rx3 LOS flag mask | Masking bit for Rx LOS flag, media lane 3 | |
| | 1 | M-Rx2 LOS flag mask | Masking bit for Rx LOS flag, media lane 2 | |
| | 0 | M-Rx1 LOS flag mask | Masking bit for Rx LOS flag, media lane 1 | |
| 227 | 7 | M-Rx8 CDR LOL flag mask | Masking bit for Rx CDR LOL flag, media lane 8 | RW Opt. |
| | 6 | M-Rx7 CDR LOL flag mask | Masking bit for Rx CDR LOL flag, media lane 7 | |
| | 5 | M-Rx6 CDR LOL flag mask | Masking bit for Rx CDR LOL flag, media lane 6 | |
| | 4 | M-Rx5 CDR LOL flag mask | Masking bit for Rx CDR LOL flag, media lane 5 | |
| | 3 | M-Rx4 CDR LOL flag mask | Masking bit for Rx CDR LOL flag, media lane 4 | |
| | 2 | M-Rx3 CDR LOL flag mask | Masking bit for Rx CDR LOL flag, media lane 3 | |
| | 1 | M-Rx2 CDR LOL flag mask | Masking bit for Rx CDR LOL flag, media lane 2 | |
| | 0 | M-Rx1 CDR LOL flag mask | Masking bit for Rx CDR LOL flag, media lane 1 | |
| 228 | 7 | M-Rx8 Power High Alarm flag mask | Masking bit for Rx input power High Alarm, media lane 8 | RW Opt. |
| | 6 | M-Rx7 Power High Alarm flag mask | Masking bit for Rx input power High Alarm, media lane 7 | |
| | 5 | M-Rx6 Power High Alarm flag mask | Masking bit for Rx input power High Alarm, media lane 6 | |
| | 4 | M-Rx5 Power High Alarm flag mask | Masking bit for Rx input power High Alarm, media lane 5 | |
| | 3 | M-Rx4 Power High Alarm flag mask | Masking bit for Rx input power High Alarm, media lane 4 | |
| | 2 | M-Rx3 Power High Alarm flag mask | Masking bit for Rx input power High Alarm, media lane 3 | |
| | 1 | M-Rx2 Power High Alarm flag mask | Masking bit for Rx input power High Alarm, media lane 2 | |
| | 0 | M-Rx1 Power High Alarm flag mask | Masking bit for Rx input power High Alarm, media lane 1 | |
| 229 | 7 | M-Rx8 Power Low Alarm flag mask | Masking bit for Rx input power low Alarm, media lane 8 | RW Opt. |
| | 6 | M-Rx7 Power Low Alarm flag mask | Masking bit for Rx input power low Alarm, media lane 7 | |
| | 5 | M-Rx6 Power Low Alarm flag mask | Masking bit for Rx input power low Alarm, media lane 6 | |
| | 4 | M-Rx5 Power Low Alarm flag mask | Masking bit for Rx input power low Alarm, media lane 5 | |
| | 3 | M-Rx4 Power Low Alarm flag mask | Masking bit for Rx input power low Alarm, media lane 4 | |
| | 2 | M-Rx3 Power Low Alarm flag mask | Masking bit for Rx input power low Alarm, media lane 3 | |
| | 1 | M-Rx2 Power Low Alarm flag mask | Masking bit for Rx input power low Alarm, media lane 2 | |
| | 0 | M-Rx1 Power Low Alarm flag mask | Masking bit for Rx input power low Alarm, media lane 1 | |

| | | | | |
|---|---|---|---|---|
| 230 | 7 | M-Rx8 Power High Warning flag mask | Masking bit for Rx input power High Warning, media lane 8 | RW Opt. |
| | 6 | M-Rx7 Power High Warning flag mask | Masking bit for Rx input power High Warning, media lane 7 | |
| | 5 | M-Rx6 Power High Warning flag mask | Masking bit for Rx input power High Warning, media lane 6 | |
| | 4 | M-Rx5 Power High Warning flag mask | Masking bit for Rx input power High Warning, media lane 5 | |
| | 3 | M-Rx4 Power High Warning flag mask | Masking bit for Rx input power High Warning, media lane 4 | |
| | 2 | M-Rx3 Power High Warning flag mask | Masking bit for Rx input power High Warning, media lane 3 | |
| | 1 | M-Rx2 Power High Warning flag mask | Masking bit for Rx input power High Warning, media lane 2 | |
| | 0 | M-Rx1 Power High Warning flag mask | Masking bit for Rx input power High Warning, media lane 1 | |
| 231 | 7 | M-Rx8 Power Low Warning flag mask | Masking bit for Rx input power Low Warning, media lane 8 | RW Opt. |
| | 6 | M-Rx7 Power Low Warning flag mask | Masking bit for Rx input power Low Warning, media lane 7 | |
| | 5 | M-Rx6 Power Low Warning flag mask | Masking bit for Rx input power Low Warning, media lane 6 | |
| | 4 | M-Rx5 Power Low Warning flag mask | Masking bit for Rx input power Low Warning, media lane 5 | |
| | 3 | M-Rx4 Power Low Warning flag mask | Masking bit for Rx input power Low Warning, media lane 4 | |
| | 2 | M-Rx3 Power Low Warning flag mask | Masking bit for Rx input power Low Warning, media lane 3 | |
| | 1 | M-Rx2 Power Low Warning flag mask | Masking bit for Rx input power Low Warning, media lane 2 | |
| | 0 | M-Rx1 Power Low Warning flag mask | Masking bit for Rx input power Low Warning, media lane 1 | |

| Byte | Bits | Name | Description | Type |
|---|---|---|---|---|
| 31 | 7 | M-CDB Block 2 | Masking bit for CDB Block 2 Complete flag | RW |
| | | complete | | Opt. |
| | 6 | M-CDB Block 1 complete | Masking bit for CDB Block 1 Complete flag | RW Opt. |
| | 5-3 | Reserved | | RO |
| | 2 | M-Data Path firmware fault | Masking bit for Data Path Firmware Fault flag | RW Opt. |
| | 1 | M-Module firmware fault | Masking bit for Module Firmware Fault flag | RW Opt. |
| | 0 | M-Module State changed flag mask | Masking bit for Module State Changed flag | RW RQD |
| 32 | 7 | M-Vcc3.3 Low Warning flag mask | Masking bit for Vcc3.3 monitor low warning flag | RW Opt. |
| | 6 | M-Vcc3.3 High Warning flag mask | Masking bit for Vcc3.3 monitor high warning flag | |
| | 5 | M-Vcc3.3 Low Alarm flag mask | Masking bit for Vcc3.3 monitor low alarm flag | |
| | 4 | M-Vcc3.3 High Alarm flag mask | Masking bit for Vcc3.3 monitor high alarm flag | |
| | 3 | M-Temp Low Warning flag mask | Masking bit for temperature monitor low warning flag | |
| | 2 | M-Temp High Warning flag mask | Masking bit for temperature monitor high warning flag | |
| | 1 | M-Temp Low Alarm flag mask | Masking bit for temperature monitor low alarm flag | |
| | 0 | M-Temp High Alarm flag mask | Masking bit for temperature monitor high alarm flag | |

| | | | | |
|---|---|---|---|---|
| 33 | 7 | M-Aux 2 Low Warning flag mask | Masking bit for Aux 2 monitor low warning flag | RW Opt. |
| | 6 | M-Aux 2 High Warning flag mask | Masking bit for Aux 2 monitor high warning flag | |
| | 5 | M-Aux 2 Low Alarm flag mask | Masking bit for Aux 2 monitor low alarm flag | |
| | 4 | M-Aux 2 High Alarm flag mask | Masking bit for Aux 2 monitor high alarm flag | |
| | 3 | M-Aux 1 Low Warning flag mask | Masking bit for Aux 1 monitor low warning flag | |
| | 2 | M-Aux 1 High Warning flag mask | Masking bit for Aux 1 monitor high warning flag | |
| | 1 | M-Aux 1 Low Alarm flag mask | Masking bit for Aux 1 monitor low alarm flag | |
| | 0 | M-Aux 1 High Alarm flag mask | Masking bit for Aux 1 monitor high alarm flag | |
| 34 | 7 | M-Vendor Defined Low Warning flag mask | Masking bit for Vendor defined low warning flag | RW Opt. |
| | 6 | M-Vendor Defined High Warning flag mask | Masking bit for Vendor defined high warning flag | |
| | 5 | M-Vendor Defined Low Alarm flag mask | Masking bit for Vendor defined low alarm flag | |
| | 4 | M-Vendor Defined High Alarm flag mask | Masking bit for Vendor defined high alarm flag | |
| | 3 | M-Aux 3 Low Warning flag mask | Masking bit for Aux 3 monitor low warning flag | |
| | 2 | M-Aux 3 High Warning | Masking bit for Aux 3 monitor high warning flag | |
| | | flag mask | | |
| | 1 | M-Aux 3 Low Alarm flag mask | Masking bit for Aux 3 monitor low alarm flag | |
| | 0 | M-Aux 3 High Alarm flag mask | Masking bit for Aux 3 monitor high alarm flag | |
| 35 | 7-0 | Reserved flag mask | | |
| 36 | 7-0 | Custom | Module level flag masks | |

## 4.3 Controls

The control fields allow the host to dynamically change the behavior of the device. It allows the user to control Tx Input Equalization, Rx amplitude, Rx Pre-Cursor and Rx Post-Cursor.

The User should follow this procedure:

- Set values to the control fields.
- Apply the configuration by selecting either ApplyDataPathInit or ApplyImmmediate.
- Press one of the 2 buttons (Apply All or Apply Lane) depending on user need.
- The module copies the data to the Active set.
- If the DataPathPwrUp is set, this applied configuration will be applied to the hardware.

Also this tab allows the user to control the module voltage, in case of the MCB is supplied by dual supply (5V and 3.3V). Three voltage levels are available: 3.15V, 3.3V and 3.45V.

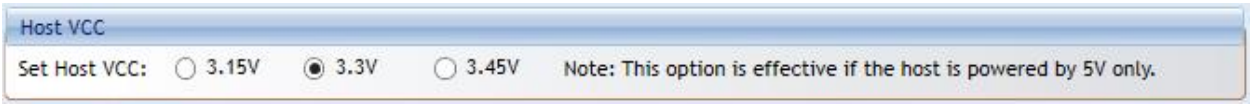


**Figure 4: MCB Voltage Control**

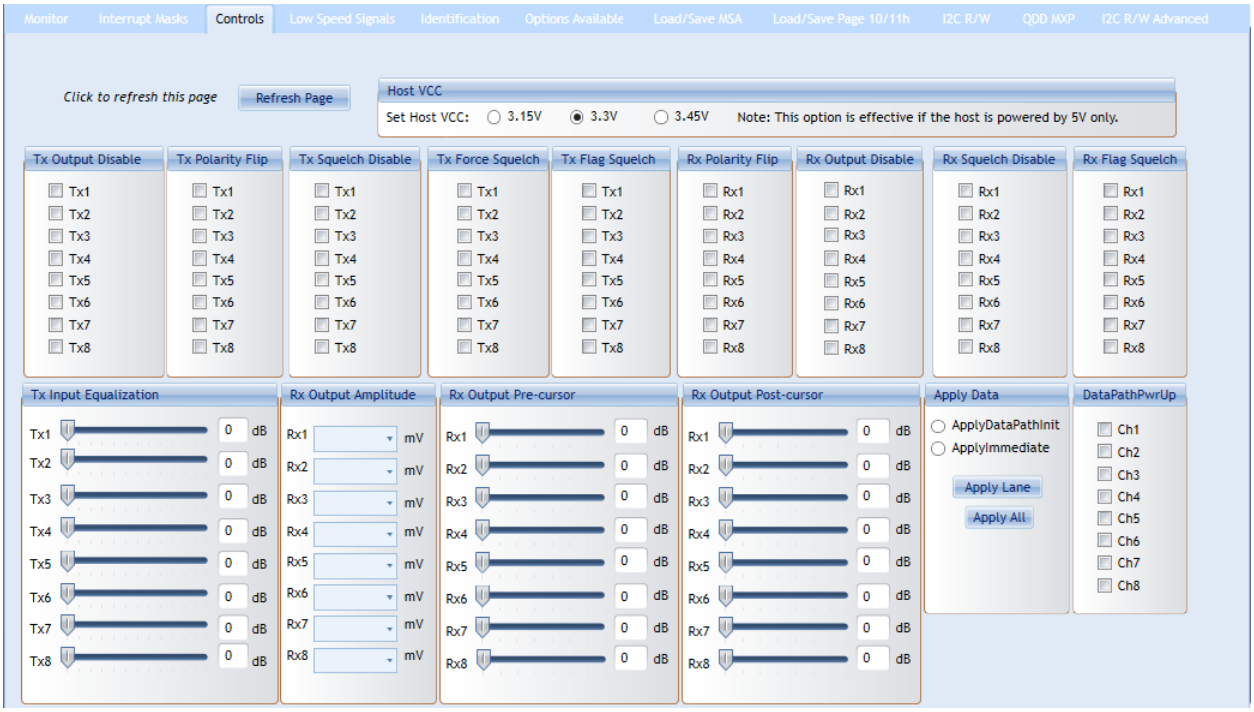


**Figure 5: Control Tab**

The following table shows the corresponding registers, along with their names and description.

| Byte | Bit | Name | Description | Type |
|---|---|---|---|---|
| 128 | 7 | DataPathDeinit Host Lane 8 | Data Path initialization control for host lane 8<br>0b=Initialize the data path associated with host lane 8<br>1b=Deinitialize the data path associated with host lane 8 | RW<br>RQD |
| | 6 | DataPathDeinit Host Lane 7 | Data Path initialization control for host lane 7<br>0b=Initialize the data path associated with host lane 7<br>1b=Deinitialize the data path associated with host lane 7 | |
| | 5 | DataPathDeinit Host Lane 6 | Data Path initialization control for host lane 6<br>0b=Initialize the data path associated with host lane 6<br>1b=Deinitialize the data path associated with host lane 6 | |
| | 4 | DataPathDeinit Host Lane 5 | Data Path initialization control for host lane 5<br>0b=Initialize the data path associated with host lane 5<br>1b= Deinitialize the data path associated with host lane 5 | |
| | 3 | DataPathDeinit Host Lane 4 | Data Path initialization control for host lane 4<br>0b=Initialize the data path associated with host lane 4<br>1b=Deinitialize the data path associated with host lane 4 | |
| | 2 | DataPathDeinit Host Lane 3 | Data Path initialization control for host lane 3<br>0b=Initialize the data path associated with host lane 4<br>1b=Deinitialize the data path associated with host lane 3 | |
| | 1 | DataPathDeinit Host Lane 2 | Data Path initialization control for host lane 2<br>0b=Initialize the data path associated with host lane 2<br>1b=Deinitialize the data path associated with host lane 2 | |
| | 0 | DataPathDeinit Host Lane 1 | Data Path initialization control for host lane 1<br>0b=Initialize the data path associated with host lane 1<br>1b=Deinitialize the data path associated with host lane 1 | |

| | | | | |
|---|---|---|---|---|
| 129 | 7 | Tx8 Polarity Flip | 0b=No polarity flip for lane 8<br>1b=Tx input polarity flip for lane 8 | RW Opt. |
| | 6 | Tx7 Polarity Flip | 0b=No polarity flip for lane 7<br>1b=Tx input polarity flip for lane 7 | |
| | 5 | Tx6 Polarity Flip | 0b=No polarity flip for lane 6<br>1b=Tx input polarity flip for lane 6 | |
| | 4 | Tx5 Polarity Flip | 0b=No polarity flip for lane 5<br>1b=Tx input polarity flip for lane 5 | |
| | 3 | Tx4 Polarity Flip | 0b=No polarity flip for lane 4<br>1b=Tx input polarity flip for lane 4 | |
| | 2 | Tx3 Polarity Flip | 0b=No polarity flip for lane 3<br>1b=Tx input polarity flip for lane 3 | |
| | 1 | Tx2 Polarity Flip | 0b=No polarity flip for lane 2<br>1b=Tx input polarity flip for lane 2 | |
| | 0 | Tx1 Polarity Flip | 0b=No polarity flip for lane 1<br>1b=Tx input polarity flip for lane 1 | |
| 130 | 7 | Tx8 Disable | 0b=Tx output enabled for media lane 8<br>1b=Tx output disabled for media lane 8 | RW Opt. |
| | 6 | Tx7 Disable | 0b=Tx output enabled for media lane 7<br>1b=Tx output disabled for media lane 7 | |
| | 5 | Tx6 Disable | 0b=Tx output enabled for media lane 6<br>1b=Tx output disabled for media lane 6 | |
| | 4 | Tx5 Disable | 0b=Tx output enabled for media lane 5<br>1b=Tx output disabled for media lane 5 | |
| | 3 | Tx4 Disable | 0b=Tx output enabled for media lane 4<br>1b=Tx output disabled for media lane 4 | |
| | 2 | Tx3 Disable | 0b=Tx output enabled for media lane 3 | |
| | | | 1b=Tx output disabled for media lane 3 | |
| | 1 | Tx2 Disable | 0b=Tx output enabled for media lane 2<br>1b=Tx output disabled for media lane 2 | |
| | 0 | Tx1 Disable | 0b=Tx output enabled for media lane 1<br>1b=Tx output disabled for media lane 1 | |
| 131 | 7 | Tx8 Squelch Disable | 0b=Tx output squelch permitted for media lane 8 when associated host input LOS is detected<br>1b=Tx output squelch not permitted for media lane 8 | RW Opt. |
| | 6 | Tx7 Squelch Disable | 0b=Tx output squelch permitted for media lane 7 when associated host input LOS is detected<br>1b=Tx output squelch not permitted for media lane 7 | |
| | 5 | Tx6 Squelch Disable | 0b=Tx output squelch permitted for media lane 6 when associated host input LOS is detected<br>1b=Tx output squelch not permitted for media lane 6 | |
| | 4 | Tx5 Squelch Disable | 0b=Tx output squelch permitted for media lane 5 when associated host input LOS is detected<br>1b=Tx output squelch not permitted for media lane 5 | |
| | 3 | Tx4 Squelch Disable | 0b=Tx output squelch permitted for media lane 4 when associated host input LOS is detected<br>1b=Tx output squelch not permitted for media lane 4 | |
| | 2 | Tx3 Squelch Disable | 0b=Tx output squelch permitted for media lane 3 when associated host input LOS is detected<br>1b=Tx output squelch not permitted for media lane 3 | |
| | 1 | Tx2 Squelch Disable | 0b=Tx output squelch permitted for media lane 2 when associated host input LOS is detected<br>1b=Tx output squelch not permitted for media lane 2 | |
| | 0 | Tx1 Squelch Disable | 0b=Tx output squelch permitted for media lane 1 when associated host input LOS is detected<br>1b=Tx output squelch not permitted for media lane 1 | |

| | | | | |
|---|---|---|---|---|
| 132 | 7 | Tx8 Force Squelch | 0b=No impact on Tx behavior for media lane 8<br>1b=Tx output squelched for media lane 8 | RW<br>Opt. |
| | 6 | Tx7 Force Squelch | 0b=No impact on Tx behavior for media lane 7<br>1b=Tx output squelched for media lane 7 | |
| | 5 | Tx6 Force Squelch | 0b=No impact on Tx behavior for media lane 6<br>1b=Tx output squelched for media lane 6 | |
| | 4 | Tx5 Force Squelch | 0b=No impact on Tx behavior for media lane 5<br>1b=Tx output squelched for media lane 5 | |
| | 3 | Tx4 Force Squelch | 0b=No impact on Tx behavior for media lane 4<br>1b=Tx output squelched for media lane 4 | |
| | 2 | Tx3 Force Squelch | 0b=No impact on Tx behavior for media lane 3<br>1b=Tx output squelched for media lane 3 | |
| | 1 | Tx2 Force Squelch | 0b=No impact on Tx behavior for media lane 2<br>1b=Tx output squelched for media lane 2 | |
| | 0 | Tx1 Force Squelch | 0b=No impact on Tx behavior for media lane 1<br>1b=Tx output squelched for media lane 1 | |
| 133 | 7:0 | Reserved | | RO |
| 134 | 7 | Tx8 Input Eq Adaptation Freeze | 0b= No impact on Tx input eq adaptation behavior for lane 8<br>1b=Tx input eq adaptation frozen at last value for lane 8 | RW<br>Opt. |
| | 6 | Tx7 Input Eq Adaptation Freeze | 0b= No impact on Tx input eq adaptation behavior for lane 7<br>1b=Tx input eq adaptation frozen at last value for lane 7 | |
| | 5 | Tx6 Input Eq Adaptation Freeze | 0b= No impact on Tx input eq adaptation behavior for lane 6<br>1b=Tx input eq adaptation frozen at last value for lane 6 | |
| | 4 | Tx5 Input Eq Adaptation Freeze | 0b= No impact on Tx input eq adaptation behavior for lane 5<br>1b=Tx input eq adaptation frozen at last value for lane 5 | |
| | 3 | Tx4 Input Eq Adaptation Freeze | 0b= No impact on Tx input eq adaptation behavior for lane 4<br>1b=Tx input eq adaptation frozen at last value for lane 4 | |
| | 2 | Tx3 Input Eq Adaptation Freeze | 0b= No impact on Tx input eq adaptation behavior for lane 3<br>1b=Tx input eq adaptation frozen at last value for lane 3 | |
| | 1 | Tx2 Input Eq Adaptation Freeze | 0b= No impact on Tx input eq adaptation behavior for lane 2<br>1b=Tx input eq adaptation frozen at last value for lane 2 | |
| | 0 | Tx1 Input Eq Adaptation Freeze | 0b= No impact on Tx input eq adaptation behavior for lane 1<br>1b=Tx input eq adaptation frozen at last value for lane 1 | |
| 135 | 7-6 | Tx4 Input Eq Adaptation Store | Tx Input Eq Adaptation Store location<br>00b=reserved<br>01b=store location 1<br>10b=store location 2<br>11b=reserved<br>See section 6.2.4.4 | WO<br>Opt. |
| | 5-4 | Tx3 Input Eq Adaptation Store | | |
| | 3-2 | Tx2 Input Eq Adaptation Store | | |
| | 1-0 | Tx1 Input Eq Adaptation Store | | |
| 136 | 7-6 | Tx8 Input Eq Adaptation Store | Tx Input Eq Adaptation Store location<br>00b=reserved<br>01b=store location 1<br>10b=store location 2<br>11b=reserved<br>See section 6.2.4.4 | WO<br>Opt. |
| | 5-4 | Tx7 Input Eq Adaptation Store | | |
| | 3-2 | Tx6 Input Eq Adaptation Store | | |
| | 1-0 | Tx5 Input Eq Adaptation Store | | |
| 137 | 7 | Rx8 Polarity Flip | 0b=No polarity flip for lane 8<br>1b=Rx output polarity flip for lane 8 | RW<br>Opt. |
| | 6 | Rx7 Polarity Flip | 0b=No polarity flip for lane 7<br>1b=Rx output polarity flip for lane 7 | |
| | 5 | Rx6 Polarity Flip | 0b=No polarity flip for lane 6<br>1b=Rx output polarity flip for lane 6 | |
| | 4 | Rx5 Polarity Flip | 0b=No polarity flip for lane 5<br>1b=Rx output polarity flip for lane 5 | |
| | 3 | Rx4 Polarity Flip | 0b=No polarity flip for lane 4<br>1b=Rx output polarity flip for lane 4 | |
| | 2 | Rx3 Polarity Flip | 0b=No polarity flip for lane 3<br>1b=Rx output polarity flip for lane 3 | |
| | 1 | Rx2 Polarity Flip | 0b=No polarity flip for lane 2<br>1b=Rx output polarity flip for lane 2 | |
| | 0 | Rx1 Polarity Flip | 0b=No polarity flip for lane 1<br>1b=Rx output polarity flip for lane 1 | |

| | | | | |
|---|---|---|---|---|
| 138 | 7 | Rx8 Output Disable | 0b=Rx output enabled for lane 8<br>1b=Rx output disabled for lane 8 | RW Opt. |
| | 6 | Rx7 Output Disable | 0b=Rx output enabled for lane 7<br>1b=Rx output disabled for lane 7 | |
| | 5 | Rx6 Output Disable | 0b=Rx output enabled for lane 6<br>1b=Rx output disabled for lane 6 | |
| | 4 | Rx5 Output Disable | 0b=Rx output enabled for lane 5<br>1b=Rx output disabled for lane 5 | |
| | 3 | Rx4 Output Disable | 0b=Rx output enabled for lane 4<br>1b=Rx output disabled for lane 4 | |
| | 2 | Rx3 Output Disable | 0b=Rx output enabled for lane 3<br>1b=Rx output disabled for lane 3 | |
| | 1 | Rx2 Output Disable | 0b=Rx output enabled for lane 2<br>1b=Rx output disabled for lane 2 | |
| | 0 | Rx1 Output Disable | 0b=Rx output enabled for lane 1<br>1b=Rx output disabled for lane 1 | |
| 139 | 7 | Rx8 Squelch Disable | 0b=Rx output squelch permitted for lane 8<br>1b=Rx output squelch not permitted for lane 8 | RW Opt. |
| | 6 | Rx7 Squelch Disable | 0b=Rx output squelch permitted for lane 7<br>1b=Rx output squelch not permitted for lane 7 | |
| | 5 | Rx6 Squelch Disable | 0b=Rx output squelch permitted for lane 6<br>1b=Rx output squelch not permitted for lane 6 | |
| | 4 | Rx5 Squelch Disable | 0b=Rx output squelch permitted for lane 5<br>1b=Rx output squelch not permitted for lane 5 | |
| | 3 | Rx4 Squelch Disable | 0b=Rx output squelch permitted for lane 4<br>1b=Rx output squelch not permitted for lane 4 | |
| | 2 | Rx3 Squelch Disable | 0b=Rx output squelch permitted for lane 3<br>1b=Rx output squelch not permitted for lane 3 | |
| | 1 | Rx2 Squelch Disable | 0b=Rx output squelch permitted for lane 2<br>1b=Rx output squelch not permitted for lane 2 | |
| | 0 | Rx1 Squelch Disable | 0b=Rx output squelch permitted for lane 1<br>1b=Rx output squelch not permitted for lane 1 | |

The optional controls follow this flow diagram.

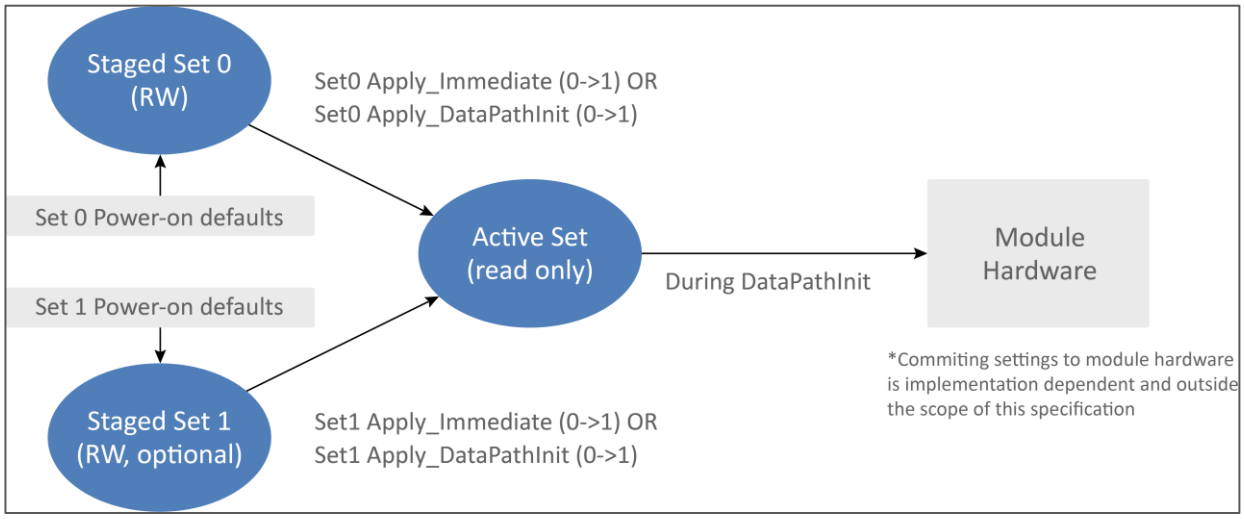


**Figure 6: Control Set Data Flow Diagram**

| | | | | |
|---|---|---|---|---|
| 143 | 7 | Staged Set 0 Lane 8 Apply_DataPathInit | 1b=Apply Staged Control Set 0 lane 8 settings using DataPathInit | WO RQD |
| | 6 | Staged Set 0 Lane 7 Apply_DataPathInit | 1b=Apply Staged Control Set 0 lane 7 settings using DataPathInit | |
| | 5 | Staged Set 0 Lane 6 Apply_DataPathInit | 1b=Apply Staged Control Set 0 lane 6 settings using DataPathInit | |
| | 4 | Staged Set 0 Lane 5 Apply_DataPathInit | 1b=Apply Staged Control Set 0 lane 5 settings using DataPathInit | |
| | 3 | Staged Set 0 Lane 4 Apply_DataPathInit | 1b=Apply Staged Control Set 0 lane 4 settings using DataPathInit | |
| | 2 | Staged Set 0 Lane 3 Apply_DataPathInit | 1b=Apply Staged Control Set 0 lane 3 settings using DataPathInit | |
| | 1 | Staged Set 0 Lane 2 Apply_DataPathInit | 1b=Apply Staged Control Set 0 lane 2 settings using DataPathInit | |
| | 0 | Staged Set 0 Lane 1 Apply_DataPathInit | 1b=Apply Staged Control Set 0 lane 1 settings using DataPathInit | |
| 144 | 7 | Staged Set 0 Lane 8 Apply_Immediate | 1b=Apply Staged Control Set 0 lane 8 settings with no Data Path State transitions | WO RQD |
| | 6 | Staged Set 0 Lane 7 Apply_Immediate | 1b=Apply Staged Control Set 0 lane 7 settings with no Data Path State transitions | |
| | 5 | Staged Set 0 Lane 6 Apply_Immediate | 1b=Apply Staged Control Set 0 lane 6 settings with no Data Path State transitions | |
| | 4 | Staged Set 0 Lane 5 Apply_Immediate | 1b=Apply Staged Control Set 0 lane 5 settings with no Data Path State transitions | |
| | 3 | Staged Set 0 Lane 4 Apply_Immediate | 1b=Apply Staged Control Set 0 lane 4 settings with no Data Path State transitions | |
| | 2 | Staged Set 0 Lane 3 Apply_Immediate | 1b=Apply Staged Control Set 0 lane 3 settings with no Data Path State transitions | |
| | 1 | Staged Set 0 Lane 2 Apply_Immediate | 1b=Apply Staged Control Set 0 lane 2 settings with no Data Path State transitions | |
| | 0 | Staged Set 0 Lane 1 Apply_Immediate | 1b=Apply Staged Control Set 0 lane 1 settings with no Data Path State transitions | |
| 145 | 7-4 | Staged Set 0 Lane 1 ApSel code | ApSel code from Table 8-13 or Table 8-39, lane 1 | RW RQD |
| | 3-1 | Staged Set 0 Lane 1 Data Path ID | First lane of the data path containing lane 1<br>000b=Lane 1, 001b=Lane 2, etc. | |
| | 0 | Staged Set 0 Lane 1 Explicit Control | 0b=Use Application-defined settings for lane 1<br>1b=use Staged Set 0 control values for lane 1 | |
| 146 | 7-4 | Staged Set 0 Lane 2 ApSel code | ApSel code from Table 8-13 or Table 8-39, lane 2 | RW RQD |
| | 3-1 | Staged Set 0 Lane 2 Data Path ID | First lane of the data path containing lane 2<br>000b=Lane 1, 001b=Lane 2 | |
| | 0 | Staged Set 0 Lane 2 Explicit Control | 0b=Use Application-defined settings for lane 2<br>1b=use Staged Set 0 control values for lane 2 | |
| 147 | 7-4 | Staged Set 0 Lane 3 ApSel code | ApSel code from Table 8-13 or Table 8-39, lane 3 | RW RQD |
| | 3-1 | Staged Set 0 Lane 3 Data Path ID | First lane of the data path containing lane 3<br>000b=Lane 1, 001b=Lane 2, etc. | |
| | 0 | Staged Set 0 Lane 3 Explicit Control | 0b=Use Application-defined settings for lane 3<br>1b=use Staged Set 0 control values for lane 3 | |
| 148 | 7-4 | Staged Set 0 Lane 4 ApSel code | ApSel code from Table 8-13 or Table 8-39, lane 4 | RW RQD |
| | 3-1 | Staged Set 0 Lane 4 Data Path ID | First lane of the data path containing lane 4<br>000b=Lane 1, 001b=Lane 2, etc. | |
| | 0 | Staged Set 0 Lane 4 Explicit Control | 0b=Use Application-defined settings for lane 4<br>1b=use Staged Set 0 control values for lane 4 | |
| 149 | 7-4 | Staged Set 0 Lane 5 ApSel code | ApSel code from Table 8-13 or Table 8-39, lane 5 | RW RQD |
| | 3-1 | Staged Set 0 Lane 5 Data Path ID | First lane of the data path containing lane 5<br>000b=Lane 1, 001b=Lane 2, etc. | |
| | 0 | Staged Set 0 Lane 5 Explicit Control | 0b=Use Application-defined settings for lane 5<br>1b=use Staged Set 0 control values for lane 5 | |
| 150 | 7-4 | Staged Set 0 Lane 6 ApSel code | ApSel code from Table 8-13 or Table 8-39, lane 6 | RW RQD |
| | 3-1 | Staged Set 0 Lane 6 Data Path ID | First lane of the data path containing lane 6<br>000b=Lane 1, 001b=Lane 2, etc. | |
| | 0 | Staged Set 0 Lane 6 Explicit Control | 0b=Use Application-defined settings for lane 6<br>1b=use Staged Set 0 control values for lane 6 | |

| | | | | |
|---|---|---|---|---|
| 151 | 7-4 | Staged Set 0 Lane 7 ApSel code | ApSel code from Table 8-13 or Table 8-39, lane 7 | RW RQD |
| | 3-1 | Staged Set 0 Lane 7 Data Path ID | First lane of the data path containing lane 7<br>000b=Lane 1, 001b=Lane 2, etc. | |
| | 0 | Staged Set 0 Lane 7 Explicit Control | 0b=Use Application-defined settings for lane 7<br>1b=use Staged Set 0 control values for lane 7 | |
| 152 | 7-4 | Staged Set 0 Lane 8 ApSel code | ApSel code from Table 8-13 or Table 8-39, lane 8 | RW RQD |
| | 3-1 | Staged Set 0 Lane 8 Data Path ID | First lane of the data path containing lane 8<br>000b=Lane 1, 001b=Lane 2, etc. | |
| | 0 | Staged Set 0 Lane 8 Explicit Control | 0b=Use Application default settings for lane 8<br>1b=use Staged Set 0 control values for lane 8 | |
| 153 | 7 | Staged Set 0 Tx8 Adaptive Input Eq Enable | 1b=Enable<br>0b=Disable (use manual fixed EQ) | RW Req |
| | 6 | Staged Set 0 Tx7 Adaptive Input Eq Enable | 1b=Enable<br>0b=Disable (use manual fixed EQ) | |
| | 5 | Staged Set 0 Tx6 Adaptive Input Eq Enable | 1b=Enable<br>0b=Disable (use manual fixed EQ) | |
| | 4 | Staged Set 0 Tx5 Adaptive Input Eq Enable | 1b=Enable<br>0b=Disable (use manual fixed EQ) | |
| | 3 | Staged Set 0 Tx4 Adaptive Input Eq Enable | 1b=Enable<br>0b=Disable (use manual fixed EQ) | |
| | 2 | Staged Set 0 Tx3 Adaptive Input Eq Enable | 1b=Enable<br>0b=Disable (use manual fixed EQ) | |
| | 1 | Staged Set 0 Tx2 Adaptive Input Eq Enable | 1b=Enable<br>0b=Disable (use manual fixed EQ) | |
| | 0 | Staged Set 0 Tx1 Adaptive Input Eq Enable | 1b=Enable<br>0b=Disable (use manual fixed EQ) | |
| 154 | 7-6 | Staged Set 0 Tx4 Adaptive Input Eq Recall | Recall stored Tx Eq adaptation value,<br>00b=do not Recall<br>01b=store location 1<br>10b=store location 2<br>11b=reserved<br>See section 6.2.4.4 for Store/Recall methodology | RW Req |
| | 5-4 | Staged Set 0 Tx3 Adaptive Input Eq Recall | | |
| | 3-2 | Staged Set 0 Tx2 Adaptive Input Eq Recall | | |
| | 1-0 | Staged Set 0 Tx1 Adaptive Input Eq Recall | | |
| 155 | 7-6 | Staged Set 0 Tx8 Adaptive Input Eq Recall | Recall stored Tx Eq adaptation value,<br>00b=do not Recall<br>01b=store location 1<br>10b=store location 2<br>11b=reserved<br>See section 6.2.4.4 for Store/Recall methodology | RW Req |
| | 5-4 | Staged Set 0 Tx7 Adaptive Input Eq Recall | | |
| | 3-2 | Staged Set 0 Tx6 Adaptive Input Eq Recall | | |
| | 1-0 | Staged Set 0 Tx5 Adaptive Input Eq Recall | | |
| 156 | 7-4 | Staged Set 0 Tx2 Input Eq control | Manual fixed Tx input eq control (See Table 6-4) | RW Req |
| | 3-0 | Staged Set 0 Tx1 Input Eq control | Manual fixed Tx input eq control (See Table 6-4) | |
| 157 | 7-4 | Staged Set 0 Tx4 Input Eq control | Manual fixed Tx input eq control (See Table 6-4) | RW Req |
| | 3-0 | Staged Set 0 Tx3 Input Eq control | Manual fixed Tx input eq control (See Table 6-4) | |
| 158 | 7-4 | Staged Set 0 Tx6 Input Eq control | Manual fixed Tx input eq control (See Table 6-4) | RW Req |
| | 3-0 | Staged Set 0 Tx5 Input Eq control | Manual fixed Tx input eq control (See Table 6-4) | |
| 159 | 7-4 | Staged Set 0 Tx8 Input Eq control | Manual fixed Tx input eq control (See Table 6-4) | RW Req |
| | 3-0 | Staged Set 0 Tx7 Input Eq control | Manual fixed Tx input eq control (See Table 6-4) | |
| 160 | 7 | Staged Set 0 Tx8 CDR control | 1b=CDR enabled, 0b=CDR bypassed | RW Req |
| | 6 | Staged Set 0 Tx7 CDR control | 1b=CDR enabled, 0b=CDR bypassed | |
| | 5 | Staged Set 0 Tx6 CDR control | 1b=CDR enabled, 0b=CDR bypassed | |
| | 4 | Staged Set 0 Tx5 CDR control | 1b=CDR enabled, 0b=CDR bypassed | |
| | 3 | Staged Set 0 Tx4 CDR control | 1b=CDR enabled, 0b=CDR bypassed | |
| | 2 | Staged Set 0 Tx3 CDR control | 1b=CDR enabled, 0b=CDR bypassed | |
| | 1 | Staged Set 0 Tx2 CDR control | 1b=CDR enabled, 0b=CDR bypassed | |
| | 0 | Staged Set 0 Tx1 CDR control | 1b=CDR enabled, 0b=CDR bypassed | |

| | | | | |
|---|---|---|---|---|
| 161 | 7 | Staged Set 0 Rx8 CDR control | 1b=CDR enabled, 0b=CDR bypassed | RW Opt. |
| | 6 | Staged Set 0 Rx7 CDR control | 1b=CDR enabled, 0b=CDR bypassed | |
| | 5 | Staged Set 0 Rx6 CDR control | 1b=CDR enabled, 0b=CDR bypassed | |
| | 4 | Staged Set 0 Rx5 CDR control | 1b=CDR enabled, 0b=CDR bypassed | |
| | 3 | Staged Set 0 Rx4 CDR control | 1b=CDR enabled, 0b=CDR bypassed | |
| | 2 | Staged Set 0 Rx3 CDR control | 1b=CDR enabled, 0b=CDR bypassed | |
| | 1 | Staged Set 0 Rx2 CDR control | 1b=CDR enabled, 0b=CDR bypassed | |
| | 0 | Staged Set 0 Rx1 CDR control | 1b=CDR enabled, 0b=CDR bypassed | |
| 162 | 7-4 | Staged Set 0 Rx2 Output Eq control, pre-cursor | Rx output equalization pre-cursor[1] | RW Opt. |
| | 3-0 | Staged Set 0 Rx1 Output Eq control, pre-cursor | Rx output equalization pre-cursor[1] | |
| 163 | 7-4 | Staged Set 0 Rx4 Output Eq control, pre-cursor | Rx output equalization pre-cursor[1] | RW Opt. |
| | 3-0 | Staged Set 0 Rx3 Output Eq control, pre-cursor | Rx output equalization pre-cursor[1] | |
| 164 | 7-4 | Staged Set 0 Rx6 Output Eq control, pre-cursor | Rx output equalization pre-cursor[1] | RW Opt. |
| | 3-0 | Staged Set 0 Rx5 Output Eq control, pre-cursor | Rx output equalization pre-cursor[1] | |
| 165 | 7-4 | Staged Set 0 Rx8 Output Eq control, pre-cursor | Rx output equalization pre-cursor[1] | RW Opt. |
| | 3-0 | Staged Set 0 Rx7 Output Eq control, pre-cursor | Rx output equalization pre-cursor[1] | |
| 166 | 7-4 | Staged Set 0 Rx2 Output Eq control, post-cursor | Rx output equalization post-cursor[1] | RW Opt. |
| | 3-0 | Staged Set 0 Rx1 Output Eq control, post-cursor | Rx output equalization post-cursor[1] | |
| 167 | 7-4 | Staged Set 0 Rx4 Output Eq control, post-cursor | Rx output equalization post-cursor[1] | RW Opt. |
| | 3-0 | Staged Set 0 Rx3 Output Eq control, post-cursor | Rx output equalization post-cursor[1] | |
| 168 | 7-4 | Staged Set 0 Rx6 Output Eq control, post-cursor | Rx output equalization post-cursor[1] | RW Opt. |
| | 3-0 | Staged Set 0 Rx5 Output Eq control, post-cursor | Rx output equalization post-cursor[1] | |
| 169 | 7-4 | Staged Set 0 Rx8 Output Eq control, post-cursor | Rx output equalization post-cursor[1] | RW Opt. |
| | 3-0 | Staged Set 0 Rx7 Output Eq control, post-cursor | Rx output equalization post-cursor[1] | |
| 170 | 7-4 | Staged Set 0 Rx2 Output Amplitude control | Rx output amplitude[2] | RW Opt. |
| | 3-0 | Staged Set 0 Rx1 Output Amplitude control | Rx output amplitude[2] | |
| 171 | 7-4 | Staged Set 0 Rx4 Output Amplitude control | Rx output amplitude[2] | RW Opt. |
| | 3-0 | Staged Set 0 Rx3 Output Amplitude control | Rx output amplitude[2] | |
| 172 | 7-4 | Staged Set 0 Rx6 Output Amplitude control | Rx output amplitude[2] | RW Opt. |
| | 3-0 | Staged Set 0 Rx5 Output Amplitude control | Rx output amplitude[2] | |
| 173 | 7-4 | Staged Set 0 Rx8 Output Amplitude control | Rx output amplitude[2] | RW Opt. |
| | 3-0 | Staged Set 0 Rx7 Output Amplitude control | Rx output amplitude[2] | |

## 4.4 Low Speed Signals

This tab allows to control and monitor the HW signals, depending on the selected device.
The sections below define the control signals for each group of devices that share the same HW signals, separately.

### 4.4.1 QDD Family

This family includes MCBs like ML4062-MCB, ML4062-MCB-MXP and ML4062-TR.

**Module Input signals:**

**LPMode:**

- If set to Low: Module is in High Power Mode
- If set to High: Module is in Low Power Mode

**ResetL:**

- If set to Low: Module is in Reset state
- If set to High: Module is out of Reset state

**ModSelL:**

- If set to Low: Module is selected and I2C communication is active
- If set to High: Module is not selected and I2C communication is inactive

**Module Output signals:**

**IntL:**

- If Read Low: interrupt source is present
- If Read High: no interrupt source is present

**ModPrsL:**

- If Read Low: Module is physically present
- If Read High: Module is physically absent

**Get** button is used to read the current state of these signals.

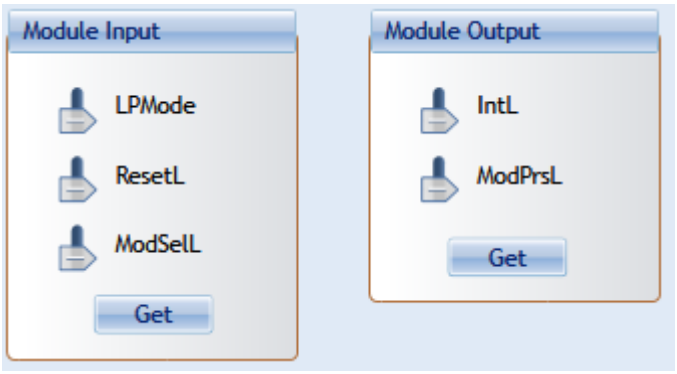


**Figure 7: QDD HW Signals**

### 4.4.2 OSFP Family

This family includes MCBs like ML4064-MCB, ML4064-TR.

**Module Input signals:**

**LPWn:**

- If set to Low: Module is in Low Power Mode
- If set to High: Module is in High Power Mode

**RSTn:**

- If set to Low: Module is in Reset State
- If set to High: Module is out of Reset State

**Module Output signals:**

**PRSn:**

- If Read Low: Module is physically present
- If Read High: Module is physically absent

**INT:**

- If Read Low: interrupt source is present
- If Read High: no interrupt source is present

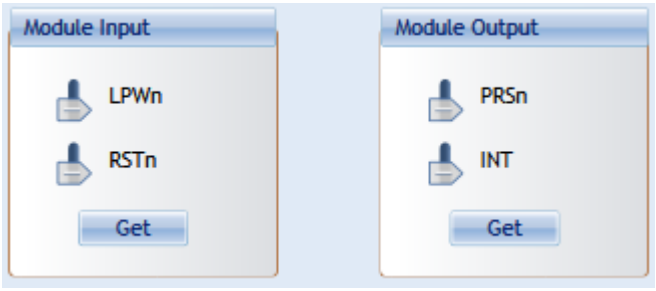


**Figure 8: OSFP HW Signals**

### 4.4.3 DSFP Family

The DSFP family includes the ML4019-MCB board.
The control signals of this family are similar to those in OSPF. Refer to section 5.4.2 for more details.

### 4.4.4 QSFP Family

This includes MCB like ML4041K.

**Module Input signals:**

**LPMode:**
- If set to Low: Module is in High Power Mode
- If set to High: Module is in Low Power Mode

**ResetL:**
- If set to Low: Module is in Reset state
- If set to High: Module is out of Reset state

**ModSelL:**
- If set to Low: Module is selected and I2C communication is active
- If set to High: Module is not selected and I2C communication is inactive

**Module Output signals:**

**IntL:**
- If Read Low: interrupt source is present
- If Read High: no interrupt source is present

**ModPrsL:**
- If Read Low: Module is physically present
- If Read High: Module is physically absent

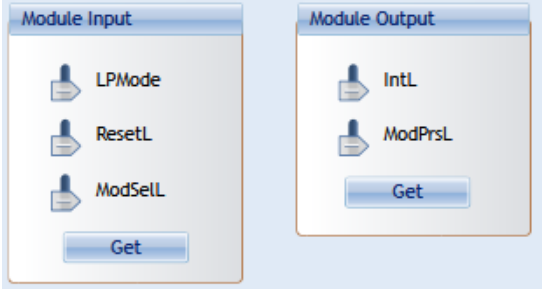


**Figure 9: QSFP HW Signals**

### 4.4.5 SFP-DD Family

This includes MCB like ML4022-MCB.

**Module Input signals:**

**LPMode:**

- If set to Low: Module is in High Power Mode
- If set to High: Module is in Low Power Mode

**TxDisable0/ TxDisable1:**

- Set to Low or High by the user for CH0 and CH1 respectively

**Module Output signals:**

**TxFault0/TxFault1:**

- Output state (Low or High) from the Module for CH0 and CH1 respectively

**RXLOS0/RXLOS1:**

- Output state (Low or High) from the Module for CH0 and CH1 respectively

User should click on **Refresh** button to get the current output signals state.

**Rate Select HW Control Contacts:**

**Speed0-1/ Speed 1-1:**

- Set the rate of the Receiver for CH0 and CH1 respectively

**Speed0-2/ Speed 1-2:**

- Set the rate of the Transmitter for CH0 and CH1 respectively

**Reserved Pins:**

**RSVD / RSVD2:**

- As Output: pins are set to High or Low
- As Input: Pins are Tri-stated

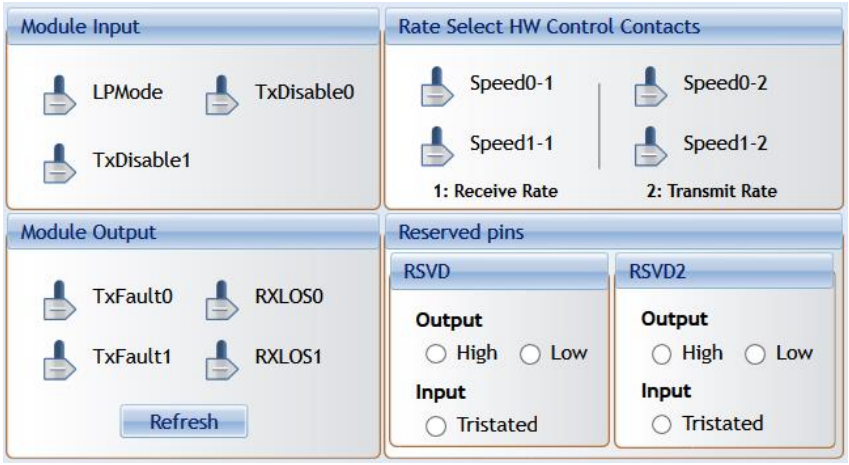


**Figure 10: SFP-DD HW Signals**

## 4.5 Identification

The Identification tab summarizes module specifications, vendor information and others.

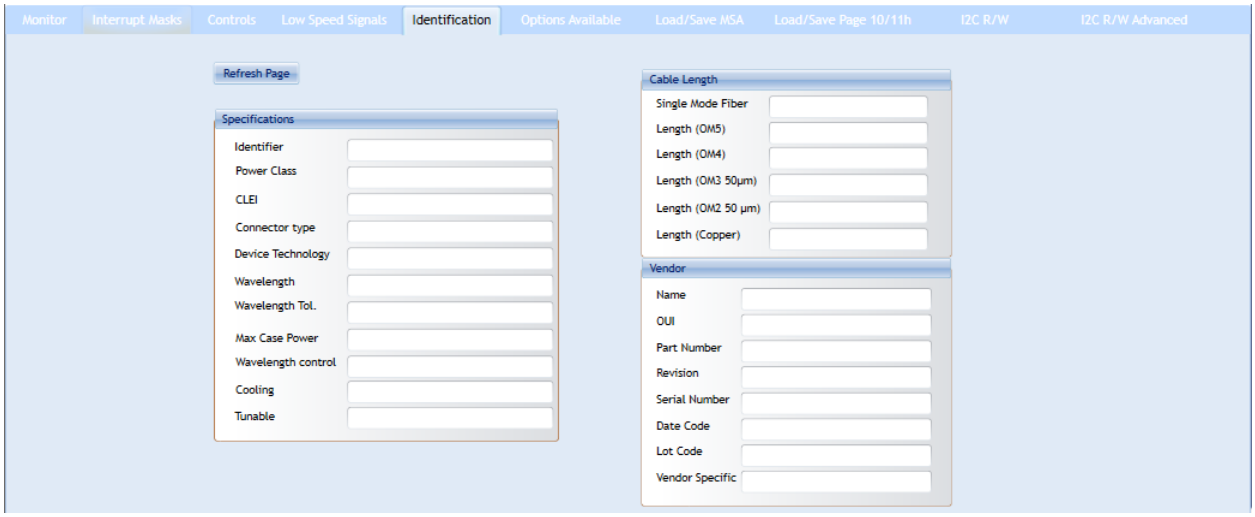


**Figure 11: Identification Tab**

The following table shows the corresponding ID registers, along with their names and description.

| Address | Size (bytes) | Name | Description |
|---|---|---|---|
| 128 | 1 | Identifier | Identifier Type of module |
| 129-144 | 16 | Vendor name | Vendor name (ASCII) |
| 145-147 | 3 | Vendor OUI | Vendor IEEE company ID |
| 148-163 | 16 | Vendor PN | Part number provided by vendor (ASCII) |
| 164-165 | 2 | Vendor rev | Revision level for part number provided by vendor (ASCII) |
| 166-181 | 16 | Vendor SN | Vendor Serial Number (ASCII) |
| 182-189 | 8 | Date Code | |
| 190-199 | 10 | CLEI code | Common Language Equipment Identification code |
| 200-201 | 2 | Module power characteristics | |
| 202 | 1 | Cable assembly length | |
| 203 | 1 | Media Connector Type | |
| 204-209 | 6 | Copper Cable Attenuation | |
| 210-211 | 2 | Cable Assembly Lane Information | |
| 212 | 1 | Media Interface Technology | |
| 213-220 | 8 | Reserved | |
| 221 | 1 | Custom | |
| 222 | 1 | Checksum | Includes bytes 128-221 |
| 223-255 | 33 | Custom Info NV | |

## 4.6 Options Available

This tab specifies the options implemented in the module.

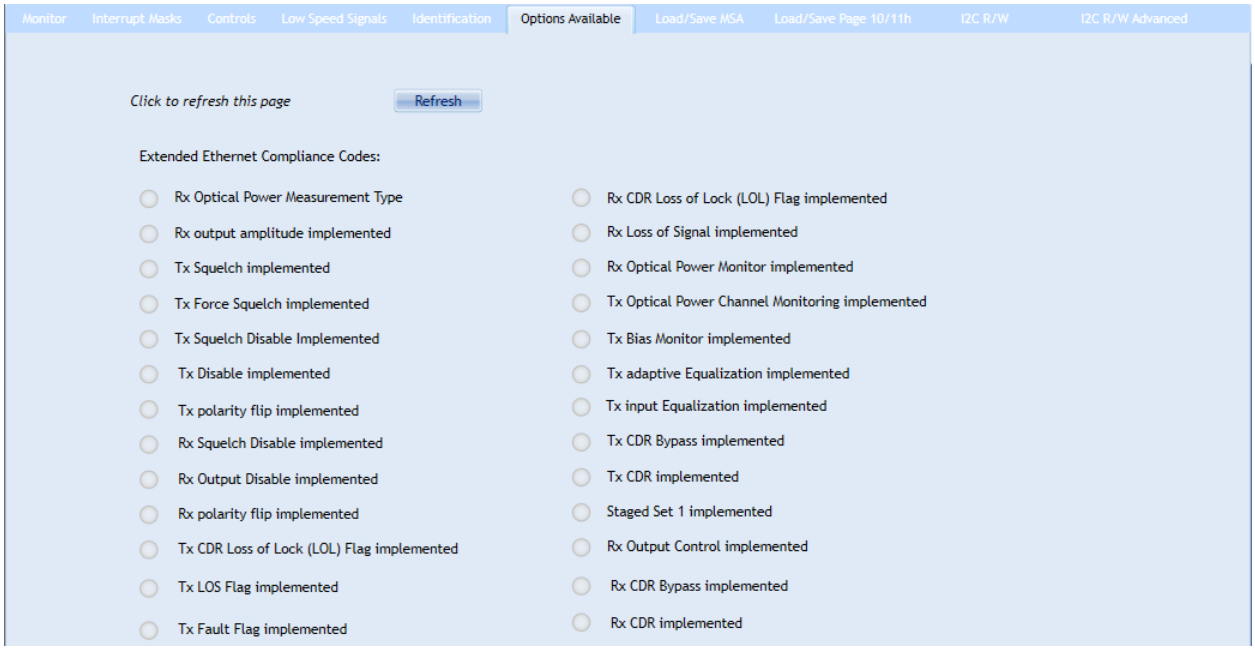


**Figure 12: Options Available Tab**

The following table shows the corresponding registers, along with their names and description.

| | | | | |
|---|---|---|---|---|
| 151 | 7 | Detector type | 0b=PIN detector<br>1b=APD detector | RO<br>RQD |
| | 6-5 | Rx Output Eq type | 00b=Peak-to-peak amplitude stays constant, or not implemented, or no information<br>01b=Steady-state amplitude stays constant<br>10b=Average of peak-to-peak and steady-state amplitude stays constant<br>11b=Reserved | |
| | 4 | Rx Optical Power Measurement type | 0b=OMA<br>1b=average power | |
| | 3 | Rx LOS type | 0b=Rx LOS responds to OMA<br>1b=Rx LOS responds to Pave | |
| | 2 | Rx LOS fast mode implemented | 0b=Rx LOS fast mode not implemented<br>1b=Rx LOS fast mode implemented<br>Refer to form factor hardware specification for timing requirements | |
| | 1 | Tx Disable fast mode implemented | 0b=Tx Disable fast mode not implemented<br>1b=Tx Disable fast mode implemented<br>Refer to form factor hardware specification for timing requirements | |
| | 0 | Module-Wide Tx Disable | 0b=Tx Disable implemented per lane<br>1b=Any Tx Disable control bit being set disables all Tx lanes | |

| | | | | |
|---|---|---|---|---|
| 152 | 7-0 | Per lane CDR Power saved | Minimum power consumption saved per CDR per lane when placed in CDR bypass in multiples of 0.01 W rounded up to the next whole multiple of 0.01 W | RO Opt. |
| 153 | 7 | Rx Output Amplitude code 0011b implemented[1] | 0b=Amplitude code 0011b not implemented<br>1b=Amplitude code 0011b implemented | RO Opt. |
| | 6 | Rx Output Amplitude code 0010b implemented[1] | 0b=Amplitude code 0010b not implemented<br>1b=Amplitude code 0010b implemented | |
| | 5 | Rx Output Amplitude code 0001b implemented[1] | 0b=Amplitude code 0001b not implemented<br>1b=Amplitude code 0001b implemented | |
| | 4 | Rx Output Amplitude code 0000b implemented[1] | 0b=Amplitude code 0000b not implemented<br>1b=Amplitude code 0000b implemented | |
| | 3-0 | Max Tx Input Eq | Maximum supported value of the Tx Input Equalization control for manual/fixed programming. (see section 6.2.4.1) | |
| 154 | 7-4 | Max Rx Output Eq Post-cursor | Maximum supported value of the Rx Output Eq Post-cursor control. (see section 6.2.4.2) | RO Opt. |
| | 3-0 | Max Rx Output Eq Pre-cursor | Maximum supported value of the Rx Output Eq Pre-cursor control (see section 6.2.4.2) | |

| Byte | Bit | Name | Description | Type |
|---|---|---|---|---|
| 155 | 7 | Wavelength control implemented | 0b=No wavelength control<br>1b=Active wavelength control implemented | RO RQD |
| | 6 | Tunable transmitter implemented | 0b=Transmitter not tunable<br>1b=Transmitter tunable (page 04h and bank page 12h shall be implemented) | |
| | 5-4 | Tx Squelch implemented | 00b=Tx Squelch not implemented<br>01b=Tx Squelch reduces OMA<br>10b=Tx Squelch reduces Pave<br>11b=User control, both OMA and Pave squelch supported. (see Table 8-7) | |
| | 3 | Tx Force Squelch implemented | 0b=Tx Force Squelch not implemented<br>1b=Tx Force Squelch implemented | |
| | 2 | Tx Squelch Disable implemented | 0b=Tx Squelch Disable not implemented | |

| Byte | Bit | Name | Description | Type |
|---|---|---|---|---|
| | | | 1b=Tx Squelch Disable implemented | |
| | 1 | Tx Disable implemented | 0b=Tx Disable not implemented<br>1b=Tx Disable implemented | |
| | 0 | Tx Polarity Flip implemented | 0b=Tx Polarity Flip not implemented<br>1b=Tx Polarity Flip implemented | |
| 156 | 7-3 | Reserved | | RO RQD |
| | 2 | Rx Squelch Disable implemented | 0b=Rx Squelch Disable not implemented<br>1b=Rx Squelch Disable implemented | RO RQD |
| | 1 | Rx Disable implemented | 0b=Rx Disable not implemented<br>1b=Rx Disable implemented | |
| | 0 | Rx Polarity Flip implemented | 0b=Rx Polarity Flip not implemented<br>1b=Rx Polarity Flip implemented | |
| 157 | 7-4 | Reserved | | RO RQD |
| | 3 | Tx Adaptive Input Eq Failflag implemented | 0b=Tx Adaptive Input Eq Fail flag not implemented<br>1b=Tx Adaptive Input Eq Fail flag implemented | RO RQD |
| | 2 | Tx CDR LOL flag implemented | 0b=Tx CDR Loss of Lock flag not implemented<br>1b=Tx CDR Loss of Lock flag implemented | |
| | 1 | Tx LOS flag implemented | 0b=Tx Loss of Signal flag not implemented<br>1b=Tx Loss of Signal flag implemented | |
| | 0 | Tx Fault flag implemented | 0b=Tx Fault flag not implemented<br>1b=Tx Fault flag implemented | |
| 158 | 7-3 | Reserved | | RO RQD |
| | 2 | Rx LOL flag implemented | 0b=Rx CDR Loss of Lock flag not implemented<br>1b=Rx CDR Loss of Lock flag implemented | RO RQD |
| | 1 | Rx LOS flag implemented | 0b=Rx Loss of Signal flag not implemented<br>1b=Rx Loss of Signal flag implemented | |
| | 0 | Reserved | | RO |

| Byte | Bit | Name | Description | Type |
|---|---|---|---|---|
| 159 | 7-6 | Reserved | | RO RQD |
| | 5 | Custom monitor implemented | 0b=Custom monitor not implemented<br>1b=Custom monitor implemented | RO RQD |
| | 4 | Aux 3 monitor implemented | 0b=Aux 3 monitor not implemented<br>1b=Aux 3 monitor implemented | |
| | 3 | Aux 2 monitor implemented | 0b=Aux 2 monitor not implemented<br>1b=Aux 2 monitor implemented | |
| | 2 | Aux 1 monitor implemented | 0b=Aux 1 monitor not implemented<br>1b=Aux 1 monitor implemented | |
| | 1 | Internal 3.3 Volts monitor implemented | 0b=Internal 3.3 V monitor not implemented<br>1b=Internal 3.3 V monitor implemented | |
| | 0 | Temperature monitor implemented | 0b=Temperature monitor not implemented<br>1b=Temperature monitor implemented | |
| 160 | 7-5 | Reserved | | RO RQD |
| | 4-3 | Tx Bias current measurement and threshold multiplier | Multiplier for 2uA Bias current increment used in Tx Bias current monitor and threshold registers (see Table 8-42 and Table 8-62)<br>00b=multiply x1<br>01b=multiply x2<br>10b=multiply x4<br>11b=reserved | |
| | 2 | Rx Optical Input Power monitor implemented | 0b=Rx Optical Input Power monitor not implemented<br>1b=Rx Optical Input Power monitor implemented | |
| | 1 | Tx Output Optical Power monitor implemented | 0b=Tx Output Optical Power monitor not implemented<br>1b=Tx Output Optical Power monitor implemented | |
| | 0 | Tx Bias monitor implemented | 0b=Tx Bias monitor not implemented<br>1b=Tx Bias monitor implemented | |
| 161 | 7 | Reserved | | RO RQD |
| | 6-5 | Tx Input Eq Store/Recall buffer count | 00b=Tx Input Eq Store/Recall not implemented<br>01b=Tx Input Eq Store/Recall buffer count=1<br>10b=Tx Input Eq Store/Recall buffer count=2<br>11b=reserved | RO RQD |
| | 4 | Tx Input Eq Freeze implemented | 0b=Tx Input Eq Freeze not implemented<br>1b=Tx Input Eq Freeze implemented | |
| | 3 | Adaptive Tx Input Eq implemented | 0b=Adaptive Tx Input Eq not implemented<br>1b=Adaptive Tx Input Eq implemented | |
| | 2 | Tx Input Eq fixed manual control implemented | 0b=Tx Input Eq Fixed Manual control not implemented<br>1b=Tx Input Eq Fixed Manual control implemented | |
| | 1 | Tx CDR Bypass control implemented | 0b=Tx CDR Bypass control not implemented (if CDR is implemented, it will be enabled)<br>1b=Tx CDR Bypass control implemented | |
| | 0 | Tx CDR implemented | 0b=Tx CDR not implemented<br>1b=Tx CDR implemented | |
| 162 | 7-6 | Reserved | | RO RQD |
| | 5 | Staged Set 1 implemented | Staged Control Set 1 implemented on Page 10h | RO RQD |
| | 4-3 | Rx Output Eq control implemented | 00b=Rx Output Eq control not implemented<br>01b=Rx Output Eq Pre-cursor control implemented<br>10b=Rx Output Eq Post-cursor control implemented<br>11b=Rx Output Eq Pre- and Post-cursor control implemented | |
| | 2 | Rx Output Amplitude control | 0b=Rx Output Amplitude control not implemented | |
| | | implemented | 1b=Rx Output Amplitude control implemented | |
| | 1 | Rx CDR Bypass control implemented | 0b=Rx CDR Bypass control not implemented (if CDR is implemented, it will be enabled)<br>1b=Rx CDR Bypass control implemented | |
| | 0 | Rx CDR implemented | 0b=Rx CDR not implemented<br>1b=Rx CDR implemented | |

## 4.7 Load/Save MSA

This tab allows the user to Load or Save his custom MSA configuration.
Data is displayed in a grid showing: register address, hex value, Decimal Values, ASCII value, MSA description.
Also the buttons available in this tab are summarized below:

- **Refresh Page**: Read MSA Registers, and refresh values.
- **Write MSA to HW**: Write the current MSA configuration to the module.
- **Save MSA to file**: Save the current MSA memory to a file using Comma separated values (CSV) format.
- **Load MSA from file**: Load MSA values from file and map it to MSA memory.
- **Checksum** for pages 00, 01 and 02

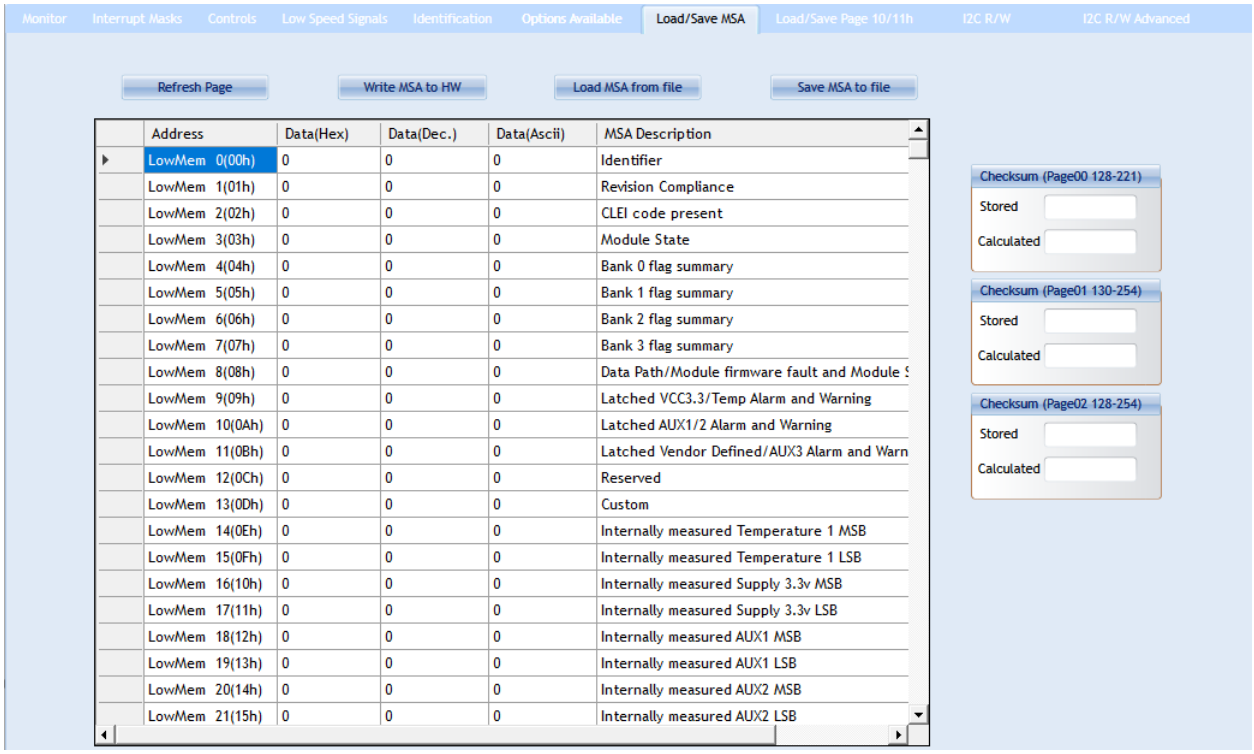


**Figure 13: Load/Save MSA Tab**

## 4.8 Load/Save Page 10/11h

This tab allows the user to Load or Save configuration for Page10h and Page11h.
Data is displayed in a grid showing: register address, hex value, Decimal Values, ASCII value and MSA description. Buttons in this tab are described below:

- **Refresh Page**: Read Registers, and refresh values.
- **Write MSA to HW**: Write the current MSA configuration to the module.
- **Save MSA to file**: saves the current MSA memory to a file using Comma separated values (CSV) format.
- **Load MSA from file**: Loads MSA values from file and map it to MSA memory.

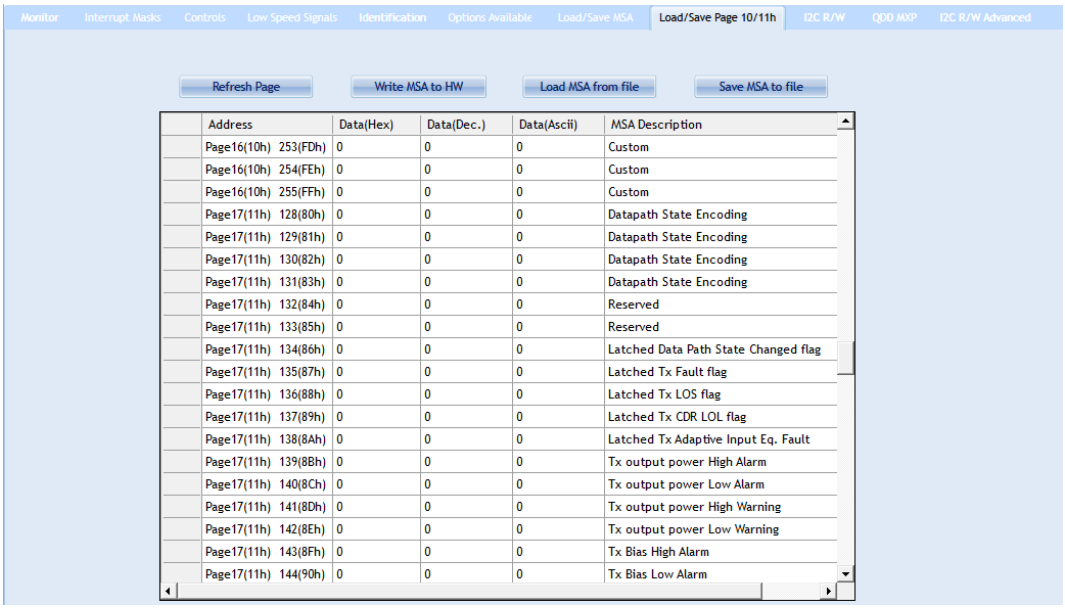


**Figure 14: Load/Save Page 10/11h Tab**

## 4.9 I2C R/W

This tab gives access to MSA registers.

1. Select the page in the **Memory Location**.
2. **Single Byte** window: to read/write one byte from the memory.
    a. Address: The address to read/write from.
    b. Memory Content: The data value read from or written to the selected address.
3. **Multi-bytes** window: to read multiple bytes between selected Starting Address and an End Address.

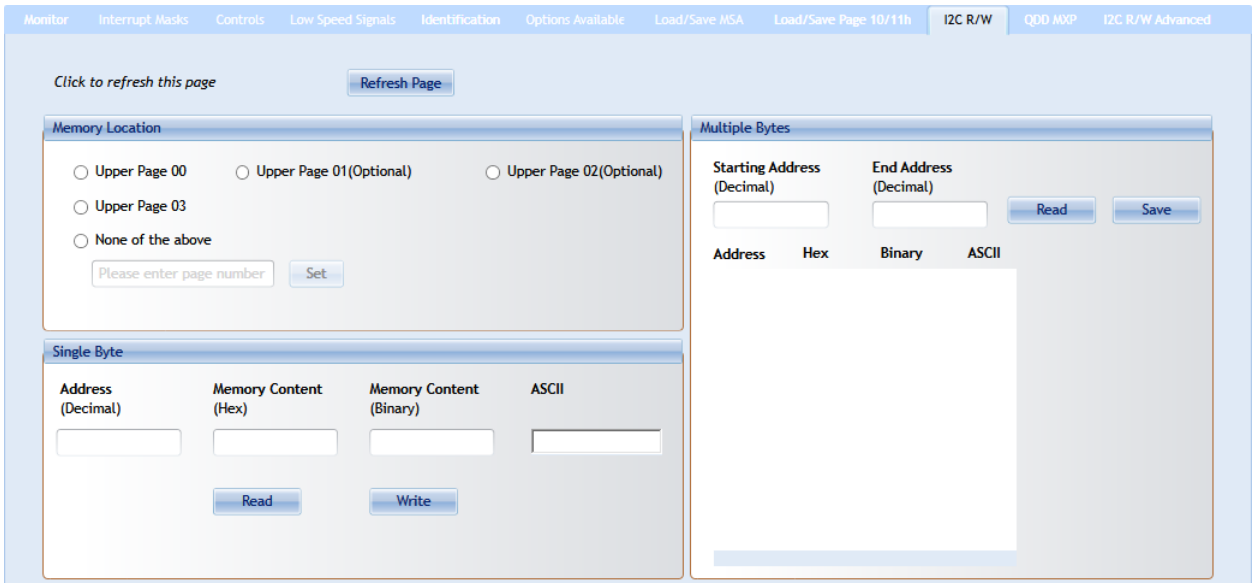


**Figure 15: I2C R/W Tab**

## 4.10 QDD MXP

**This tab is used only with ML4062-MCB-MXP.**
The following tab allows the user to modify the DC Level within a range between 3.0 and 3.6, and to insert noise to the VCC by adding noise frequency between 0 and 12500000 Hz and control noise amplitude ranging from 0 to 120mV.
Two buttons are available under Noise Insertion Window:

1. **Apply**: this must be pressed so the noise frequency and amplitude take effect
2. **Reset**: this will set noise frequency and amplitude back to 0

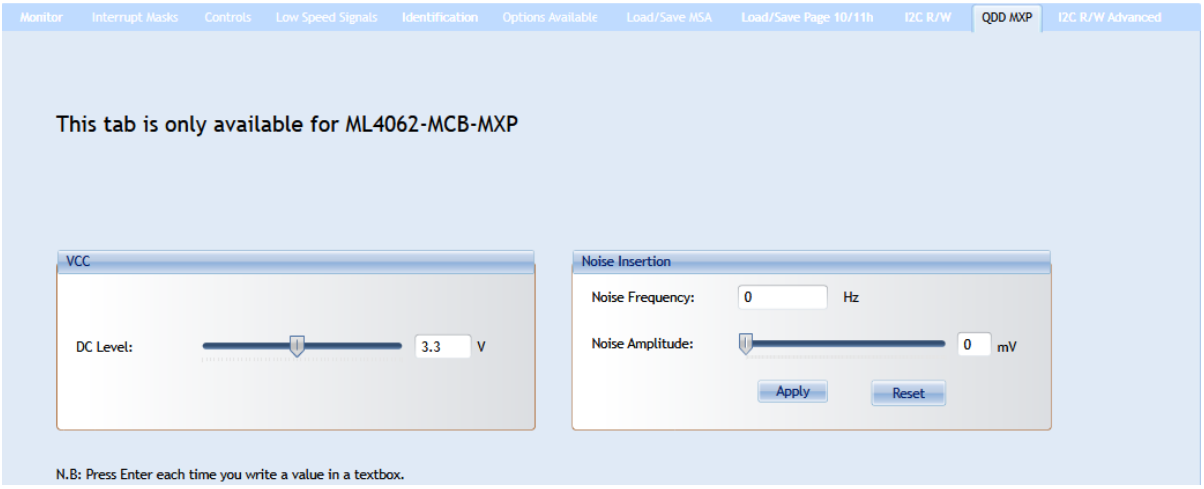


**Figure 16: QDD MXP Tab**

## 4.11 I2C R/W Advanced

This tab gives access to MSA registers without specifying the Slave address.

1. Select **Page Number** under **Memory Location** window.
2. Under **Single Byte** window.
    - Write the corresponding **Slave Address**
    - Write the **Address** to read from or write to
    - Data to be written to or Read from the selected address is under **Memory Content** field
3. Under **Multi-Byte Read** window.
    - Write the corresponding **Slave Address**
    - Select the **Starting Address** and the **End Address** to Read from

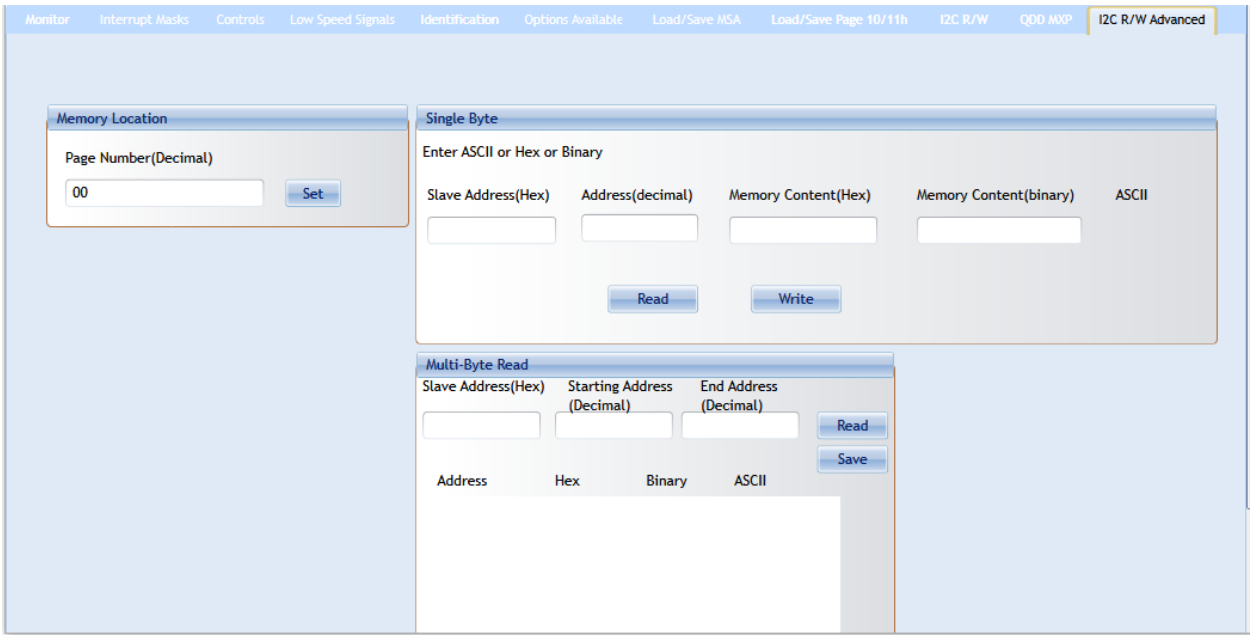


**Figure 17: I2C R/W Advanced Tab**

## 4.12 Command Data Block (CDB) Message Communication

The Common Data Block (CDB) is a message communication protocol between the Host and a Module that allows the user to check and apply various settings on the interconnect, including updating the firmware. CDB is a Two Wire serial Interface (TWI) protocol based on the i2c for CMIS 4.0 and 5.0 between a Master (Initiator in 5.0) and Slave (Target in 5.0).
The host sends a CDB Command (CMD) message which is identified by a CMD ID and the module responds with a CDB Reply (REPLY) message without changing the CMD ID.
On the ML4062 Module Compliance Board (MCB), the CDB enables the issuing of commands from the MCB to the interconnect. The ML4062 MCB includes all CDB commands mentioned in CMIS 4.0 and CMIS 5.0.

Unlock CDB feature by loading the purchased License File:

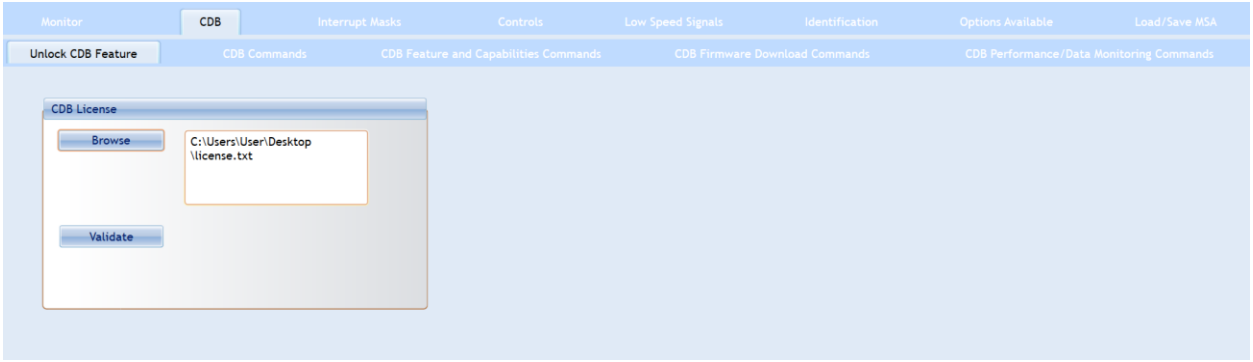


**Figure 21: CDB License Validation**

### 4.12.1 CDB Commands

- **CMD 0000h Query Status**
- **CMD 0001h Enter Password**
- **CMD 0002h Change Password**
- **CMD 0003h Enable/Disable Password Protection**
- **CMD 0004h General Abort**
- **CMD 0380h Loopbacks**

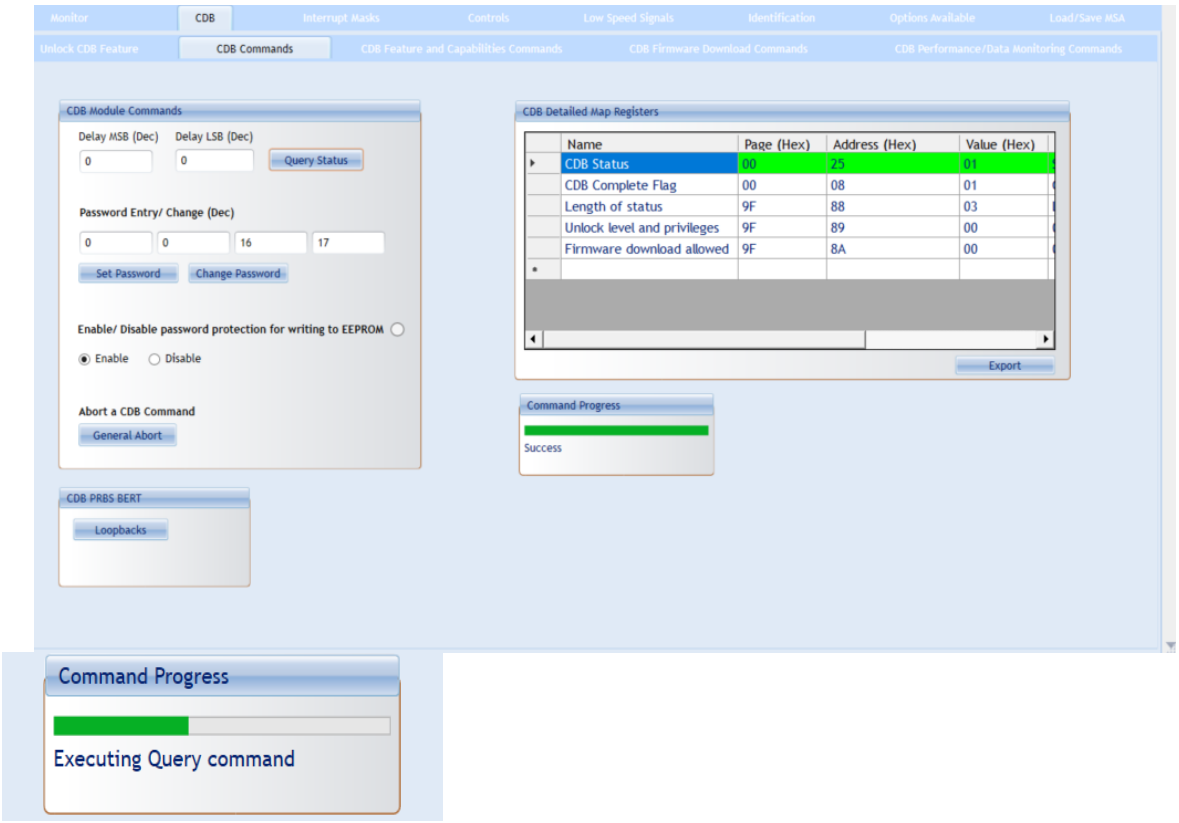


**Figure 22: CDB Commands**

The CDB GUI includes detailed map registers that show what is returned by each command.
Here, for example, the query status command is being sent. A progress bar indicates the progress of the running CDB command. The GUI clearly indicates that the command was sent successfully (CDB status=1), that it asserts the CDB flag, and that it returns three bytes of data as shown with the corresponding value and description. The User can export this data (to an excel sheet) using the export button.

### 4.12.2 CDB Feature and Capabilities Commands

- **CMD 0040h Module Features**: Identifies which commands are supported, from CMD 0 to CMD 00FF along with the maximum CDB command execution time.
- **CMD 0042h Performance Monitoring**: Identifies which commands are supported from 0200h to 02FFh.
- **CMD 0043h Bert and diagnostics**: Identifies CMD 0300h to 03FFh.
- **CMD 0041h Read FW Features**: Identifies many parameters supported the firmware features including firmware download transfer type, if copy/abort/full image readback commands are supported, start command payload size, erased byte, the firmware update features, if read/write firmware is supported, the firmware can be upgraded, etc. Use this feature to determine whether a device supports LPL or EPL firmware.

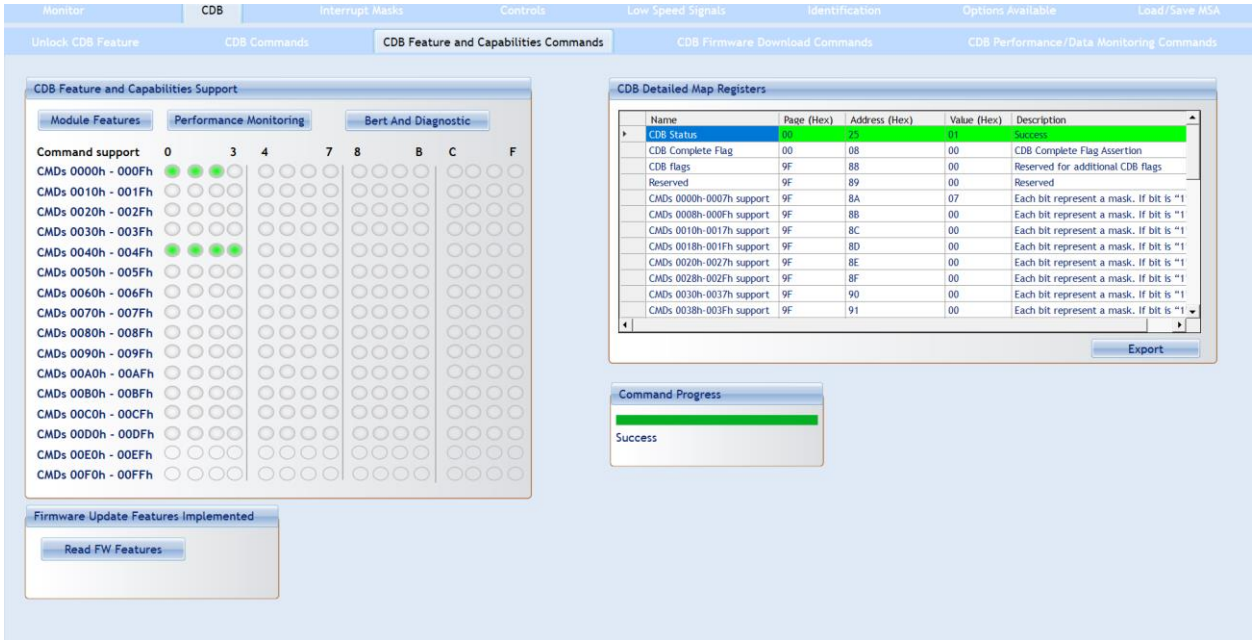


**Figure 23: CDB Feature and Capabilities Commands**

The green buttons indicate which commands are supported. In this case, the module feature command is returning the corresponding data in the detailed map register and indicates that CMDs 0,1,2,40,41,42,43 are supported (other modules might support other commands).

### 4.12.3 CDB Firmware Download Commands

- **CMD 0101h, 0103h, 0107h Program LPL**: Loads the firmware binary file for Local Payload (LPL). Allows for updating interconnect firmware.
- **CMD 0101h, 0104h, 0107h Program EPL**: Loads the firmware binary file for Extended Payload (EPL). EPL support varies depending on the interconnect. Allows for updating interconnect firmware.
- **CMD 0101h, 0105h, 0107h Read Image LPL**: Read the latest upgraded firmware image using LPL

- **CMD 0101h, 0106h, 0107h Read Image EPL**: Read the latest upgraded firmware image using EPL.
- Export Image: Exports an image of the firmware after the read is completed as a .bin file, which in turn can be loaded into and read by other interconnects.
- **CMD 0102h Abort FW download**: Stops the firmware from being installed onto the interconnect.
- **CMD 0109h Run image**: After the new LPL or EPL Firmware is loaded, this command switches to the latest firmware image. Does not replace the existing firmware image on the interconnect.
- **CMD 010Ah Commit image**: Replaces the firmware image on the interconnect with the new loaded firmware image. Prior to this command being executed, the old firmware will still be executed on startup. Always ensure the new image is running perfectly (by running it on the interconnect using the previous commands) before using this command.
- **CMD 0108h Copy image A to B/B to A**: In the event of two images being present on the same interconnect and both images are written to flash, this command makes ensures that both images are identical, with the copied image being specified in the commands as either image A to image B, or image B to image A.
- **CMD 0100h Get FW Info**: Loads the information about the latest firmware on the interconnect, for both image A and image B.

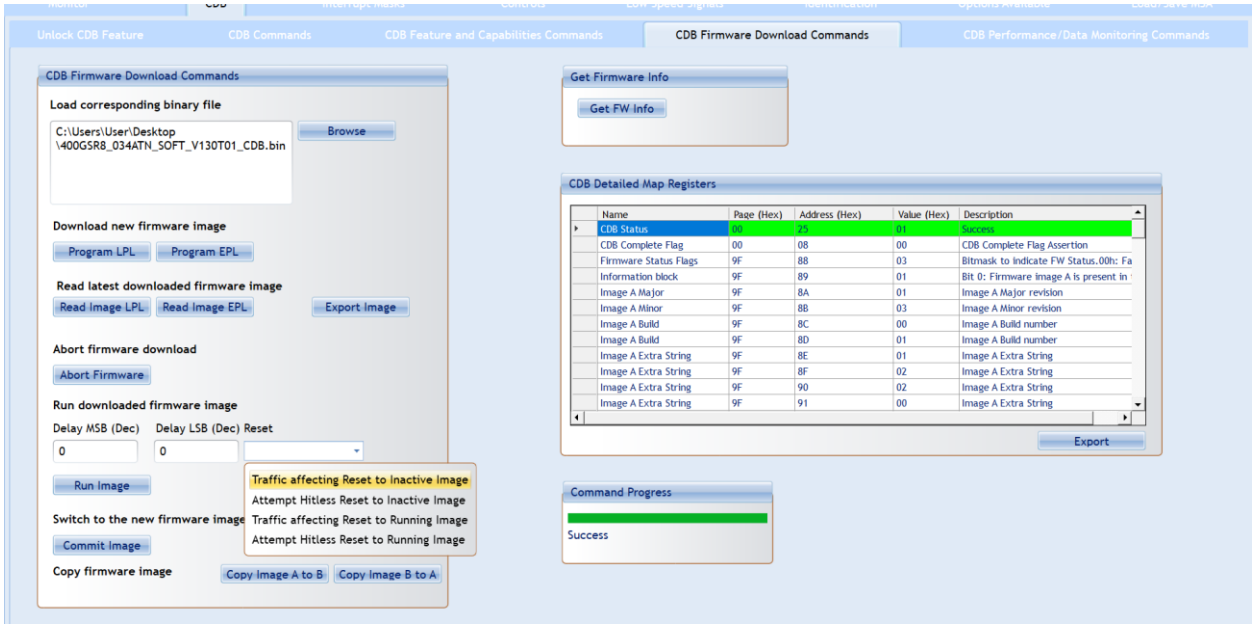


**Figure 24: CDB Firmware Download Commands**

## *4.12.4 CDB Performance/Data Monitoring Commands*

- **CMD 0200h PM Controls**: Extract Performance Monitoring data records such as minimum/average/maximum values. “No Operation” reads the most recent values, while “Clear All” clears the extracted values for all lanes in the interconnect.

- **CMD 0201h PM Feature Information**: Reads the PM's additional features.
- **CMD 0280h Data Monitoring and Recording Controls**: "Refresh" loads the most recent attributes. "Clear All" clears all values for all parameters for all lanes at the same time.
- **CMD 0281h Data monitoring and recording advertisement**
- **CMD 0290h Temperature Histogram**: Displays the temperature intervals of the interconnect and how long it stayed at each temperature interval.
- **CMD 0210h, 0211h Get Module PM LPL/EPL**: Choose parameters of the module's performance monitoring records, and replace the current values of the minimum, average, and maximum values. "Refresh" replaces the old values, while "Clear and Read" reads and resets the old values.
- **CMD 0212h, 0213h Get PM Host Side LPL/EPL**: Choose parameters of the host's performance monitoring records, and replace the current values of the minimum, average, and maximum values. "Refresh" replaces the old values, while "Clear and Read" reads and resets the old values.
- **CMD 0214h, 0214h Get PM Media Side LPL/EPL**: Choose parameters the performance monitoring records of specific lanes, and replace the current values of the minimum, average, and maximum values. "Refresh" replaces the old values, while "Clear and Read" reads and resets the old values.
- **CMD 0216h, 0217h Get Data Path PM LPL/EPL**: Choose the data path for specific lanes and replace the current values of the minimum, average, and maximum values. "Refresh" replaces the old values, while "Clear and Read" reads and resets the old values.

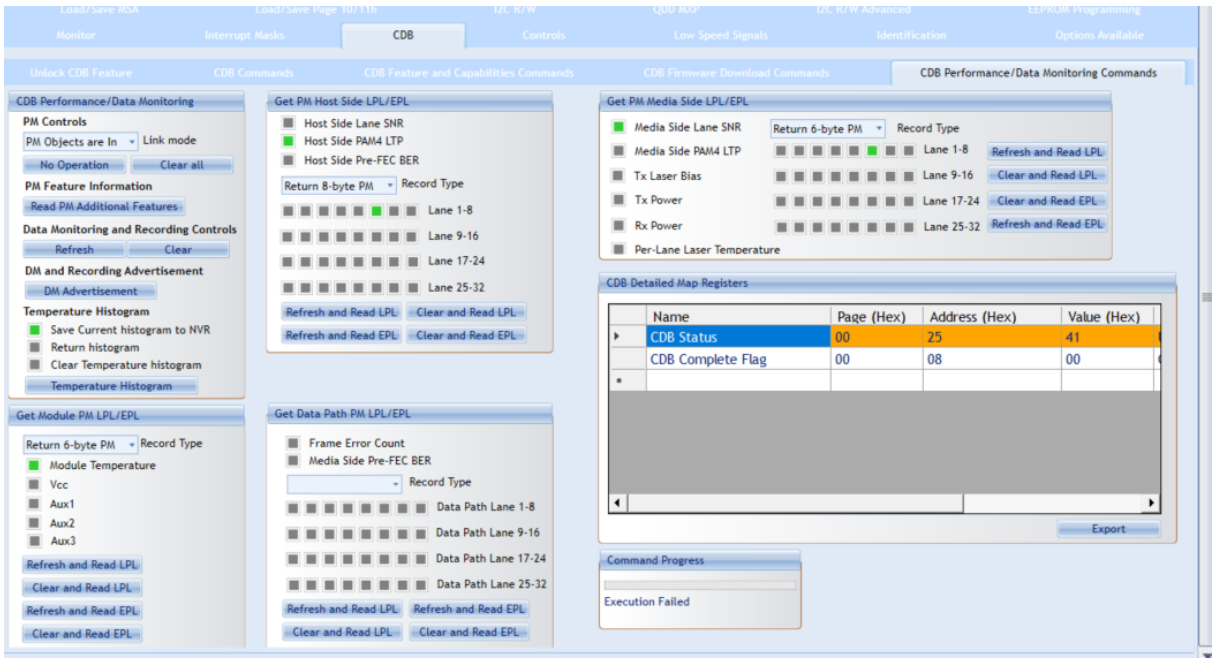


**Figure 25: CDB Performance/Data monitoring Commands**

# Software Revision

**V2.2.1:** latest Software Revision, which this document is based on.

**North America**
48521 Warm Springs Blvd. Suite 310
Fremont, CA 94539
USA
+1 510 573 6388

**Worldwide**
Houmal Technology Park
Askarieh Main Road
Houmal, Lebanon
+961 81 794 455

**Asia**
14F-5/ Rm.5, 14F., No 295
Sec.2, Guangfu Rd. East Dist.,
Hsinchu City 300, Taiwan (R.O.C)
+886 3 5744 591